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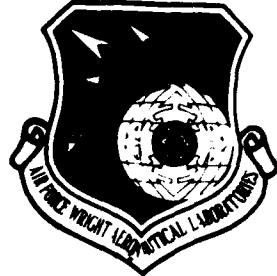
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HERMETICALLY SEALED HIGH RADIANCE LEDs FOR FIBRE OPTIC COMMUNICATIONS

R. Goodfellow
J. Humpage
R. Davis

Plessey Research (Caswell) Limited
Allen Clark Research Centre
Caswell, Towcester, Northants,
England.

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KC 7-81

K. C. TRUMBLE, Project Engineer
Information Transfer Group
Information Processing Technology Branch
System Avionics Division

Donald L. Moon

DONALD L. MOON, Chief
Information Processing Technology Branch
Avionics Laboratory

FOR THE COMMANDER

Raymond E. Siford
RAYMOND E. SIFORD, Colonel, USAF
Chief, System Avionics Division
Avionics Laboratory

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report describes the development of hermetically sealed pigtailed LEDs for Fibre Optic Communications. Hermeticity to MIL STD 7503, 1017 is achieved by a fibre metallisation/solder method, high efficiency and speed (3 nanosecs typical) by optimised GaAs-GaAlAs proton isolated junction, and high output power by microlens coupling (800μW typical in a 100μm core diameter 0.3NA pigtail).		

FOREWORD

This report described research performed under Contract No. F49620-79-C-0045 to produce hermetically sealed high radiance LED's to meet source requirements of Air Force optic data communications subsystems for space and airborne vehicles. The work was carried out at the Allen Clark Research Centre, which is the central research laboratory of the Plessey Company in England. The Programme Manager was R. Davis and key scientific personnel were: M. Faultless, R. Goodfellow, J. Humpage and J. Ure.

The period in which this research was carried out was from April 1979 to June 1980 and the report was first submitted in July 1980

An associated effort to this programme was carried out at Sandia Laboratories, Alb. N.M. by C. Barnes to determine radiation hardness of the device developed here. This was part of a larger programme performed for AFNAL to compare radiation hardness of a wide range of sources and detectors for fibre optics applications. His major finding was that the devices developed during the effort reported here were highly radiation resistant and showed the best hardness of all devices tested.

The Air Force Programme Monitor was Ken Trumble AFWAL/AAAT-3.

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1. INTRODUCTION AND BACKGROUND TECHNOLOGY

The objective of this work was to develop a fully hermetically sealed, wide temperature range, reliable, pigtailed, high radiance LED to meet source requirements of Air Force fibre optic data communications subsystems for space and airborne vehicles. The principal requirements were hermeticity to MIL Standard 750B, launch power from the pigtail fibre of $250\mu\text{W}$, with $500\mu\text{W}$ as goal and rise and fall times of 6ns with 3ns as goal, as detailed in Table 1.1. This development programme has been carried out at the Allen Clark Research Centre which is the central research laboratory of the Plessey Company in England.

The approach taken is to extend existing gallium arsenide/gallium aluminium arsenide double heterostructure materials technology to provide a LED source with the required speed-efficiency characteristics, and to enhance optical coupling to the output pigtail by optimised microlens coupling techniques. Hermetic sealing of the fibre pigtail into the LED package is accomplished by a metallisation/solder method, additionally providing a rugged and stable device configuration.⁽¹⁾

The background technology for this development is based on a surface emitting high radiance LED structure⁽²⁾ which is illustrated in Fig.1.1, this shows a GaAs device formed either by Zn diffusion or p-type epitaxial growth⁽³⁾ on an n-type GaAs substrate. The active region of the device is isolated by means of a windowed SiO_2 layer or by proton implanted semi-insulating GaAs. As part of the device fabrication process an electroplated gold heat sink is formed on the active side of the chip. This is a key factor in the technology ensuring a low thermal impedance (for high power operation) and also providing a cushioning effect when the chip is bonded to the gold plated copper stud of the package. The optical signal is extracted through the back of the chip

(1) References are given on p.78 of this report

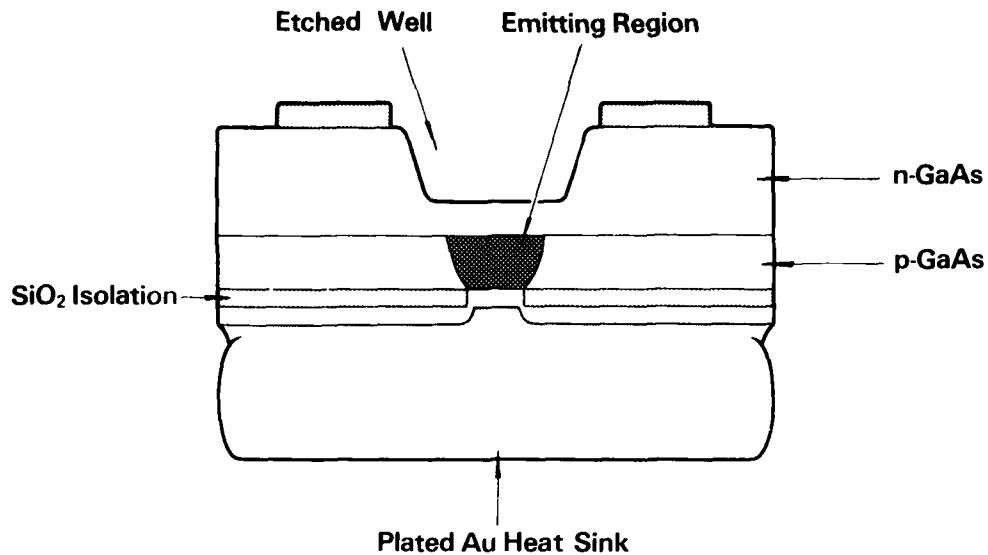


Figure 1.1

Surface Emitting High Radiance LED

TABLE 1.1

HERMETICALLY-SEALED HIGH RADIANCE LEDs FOR FIBRE OPTIC COMMUNICATIONS
SPECIFICATION

	Requirement	Goal
DC Power	250 μ W	500 μ W
Bias Current	150 mA	150 mA
Rise/Fall Time	6 ns	3 ns
Bandwidth	100 MHz	200 MHz
Temperature	-55°C/+70°C	-55°C/+125°C
Wavelength	.82-.88 μ m	
MTTF	10^5 hrs	10^6 hrs
Hermeticity	Fine and Gross per MIL-STD-750B Method 1071	

and a well is etched in the GaAs substrate so as to minimise absorption in that region.

Typical dimensions of the chip are 15 - 20 mil square with an active region of 20 - 100 microns in diameter. Devices of this type have been fabricated in GaAs for operation at 0.9 microns^(2,3), in GaAlAs⁽⁴⁾ for operation between 0.8 and 0.9 microns and in GaInAsP⁽⁵⁾ for operation between 1.0 and 1.6 microns.

One of the notable features of this device is its good life⁽⁶⁾. Results of extended life tests at the start of this programme are shown in Fig.1.2. GaAs devices had been on test at full rated power for almost five years at Plessey and had recorded 40,000 hours of actual operation. A number of factors are important in achieving long life in these devices. These include the selection criteria used in choosing the starting substrate material and carefully controlled device processing⁽⁷⁾ which ensures minimum damage to the device during chip fabrication and bonding stages.

Another aspect of the background technology which is very relevant to the development programme is the device encapsulation procedure which is illustrated in Fig.1.3. The device chip is bonded to a high conductivity copper heat sink using a Au-Sn solder. A small, truncated spherical lens is then positioned in the well of the LED to increase the coupling efficiency between the source and the fibre. This lens is fabricated of $\text{SiO}_2/\text{TiO}_2$ with a dielectric constant of 1.9. The output fibre is then held in position above the lens by soldering through the hole in the metal cap of the package. Prior to soldering the fibre is stripped of its protective coating and is metal coated by a proprietary process. This method of pigtail attachment is unique and provides a method of producing a pigtailed device which is hermetically sealed.

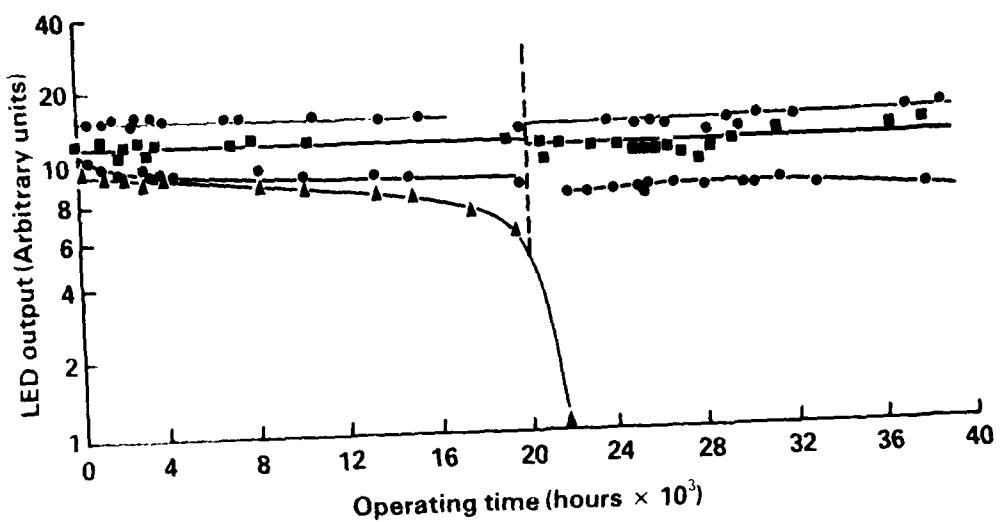


Figure 1.2
Life Test at 35°C Ambient (Begun May 1974 - 8 devices total)

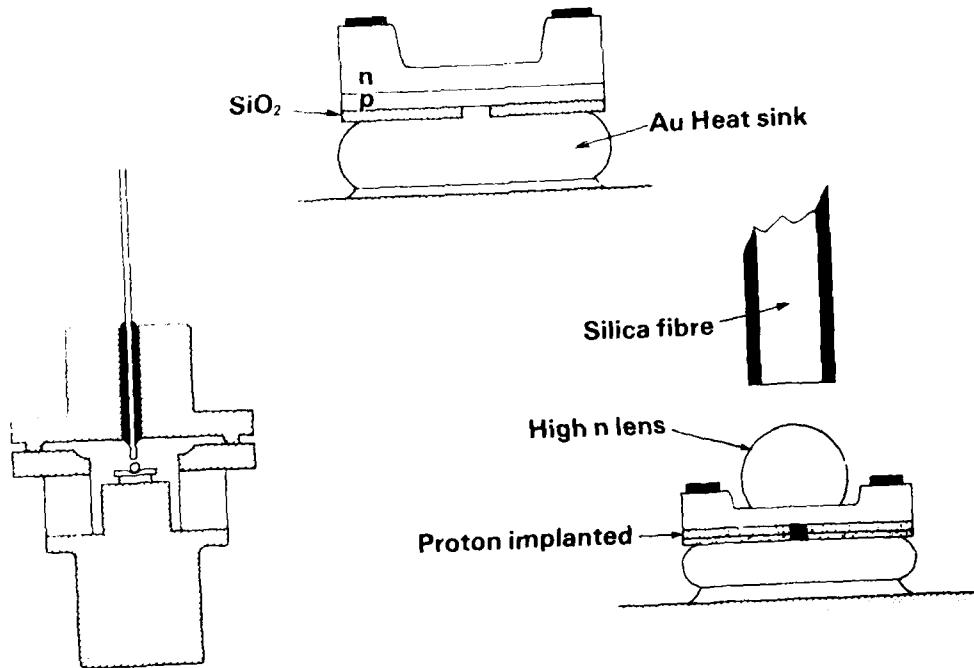


Figure 1.3

H.R. LED Assembly

It is known that there is a trade-off between power and speed in GaAs-GaAlAs LED structures; the details of this trade-off were established early in the programme in order to optimise junction design (Section 6, p.28). An initial set of experiments was carried out to establish the speed/power trade-off by deliberately varying the doping level and thickness of the active region of the device and also by fabricating devices with either oxide or proton bombardment isolation of the active region. Layers were then processed into high radiance LED structures and output power and speed of response determined. In general all wafers provided adequately high values of efficiency, so subsequent tailoring of the layer parameters was aimed at the speed requirement. The final structure was proton bombardment isolated, had a 1 μ m thick active layer doped to $4.5 \cdot 10^{18} \text{ cm}^{-3}$ with germanium and containing 5% aluminium.

The coupled power is affected by the choice of fibre numerical aperture and core diameter and a decision on the pigtail type to be used was required early in the programme in order to optimise the diode size and geometry and the lens design. The optical parameters of a number of commercially available fibres were fed into a previously established computer programme (8) which gave calculated values for optimum LED source diameter, microlens diameter and truncation and theoretical power coupling efficiency. These computations are described in Section 2, p.8. In choosing the fibre for the pigtail consideration was given to its interface with the trunking fibre and the need for proven radiation hardness in addition to the calculated coupling efficiency. The final choice for the LED pigtail was Corning SDF 100 μ m core diameter 0.3NA fibre. Our calculations, as detailed in Section 2, p.8, showed that for this fibre the LED emitting zone should be 25 μ m diameter and that a 103 μ m diameter sphere lens with 0.24 truncation factor would provide optimum coupling.

In this report we detail the work carried out to meet the contract objectives, resulting in the development of a device whose performance in terms of power and speed exceeded the goals of the contract. The ruggedness of the device, including lens attachment method, is demonstrated by survival of thermal shock testing, mechanical shock testing, and more significantly, mechanical shock testing at high temperatures. The hermeticity of the structure is proven and we believe that this marks the first time a hermetically sealed pigtailed LED has been demonstrated with good yield, approaching 80% in later batches.

2. DEVICE STRUCTURE AND LENS MODELLING

Our position at the start of the programme was that we could fabricate homojunction GaAs LED's on a production basis and we had established that these devices had good reliability with half lives around 10^5 - 10^6 hours. These devices had acceptably high efficiency and performance for many applications but this was inferior to that of GaAlAs double heterostructure devices whose reliability was yet to be established.

Fig.2.1. shows schematic cross sections of the zinc diffused GaAs homojunction LED and a GaAlAs double heterojunction (DH) LED with the typical transfer characteristics of each. This emphasises the higher efficiency of the GaAlAs DH devices which arises because carriers are confined to recombine within a well defined active region which is bounded by layers which are transparent to the generated radiation.

The fabrication procedures for homo and DH devices outlined in Fig. 2.2. differ in complexity but as a large number of chips are processed in a single batch this should have little impact on final device cost. The substrate selection step is a highly critical one in homojunction device fabrication as substrate quality affects efficiency, speed and yield.

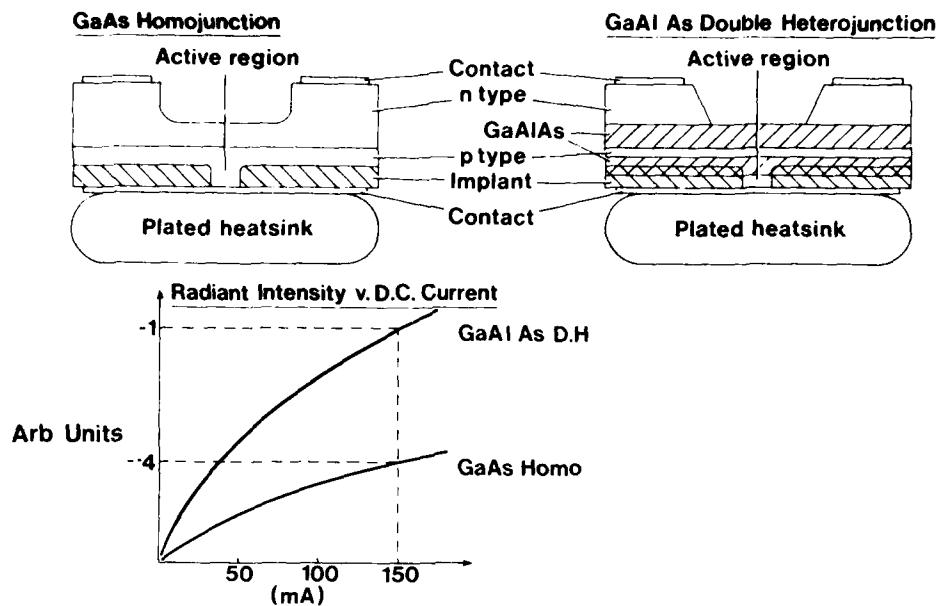


Figure 2.1
GaAs Homojunction and Double Heterojunction LEDs

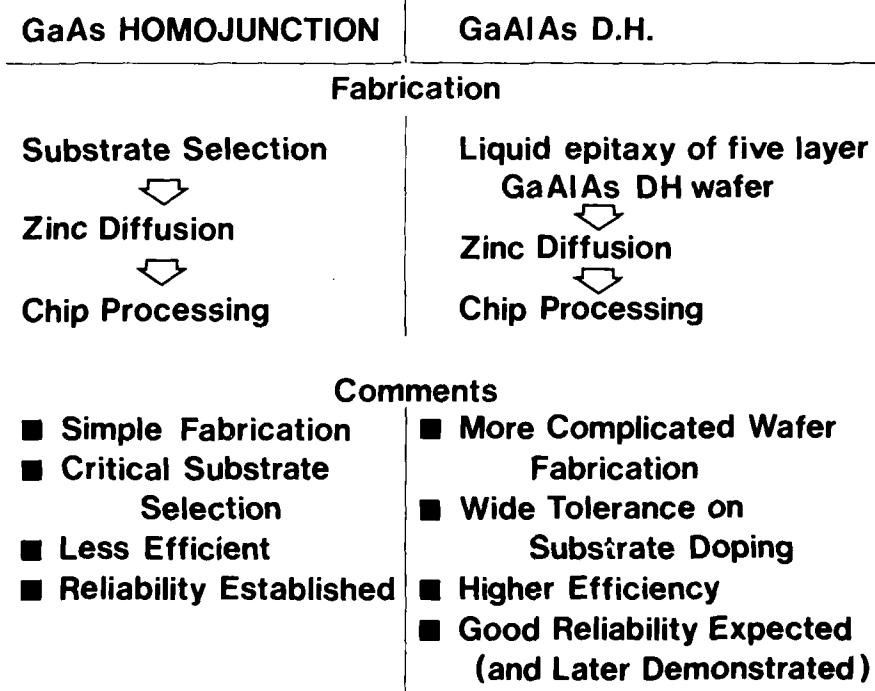


Figure 2.2
Fabrication Steps for Homo and Heterojunction LEDs

Acquisition of quantities of substrate material and rejection of a large proportion seems inevitable because of the tight acceptance tolerance.

The other procedures are relatively straightforward as detailed in Section 4, p.19. In contrast, the epitaxy step of the DH device is a critical process (as described in Section 3, p.12) but substrate selection here is based mainly on crystal perfection with a wide tolerance on donor doping concentration. Material sensitive etches can be used in the formation of the etched well to achieve better dimensional control. Good reliability was expected from the DH device and has been reasonably demonstrated in this programme with extrapolated life times in excess of 10^5 hours at 25°C . In view of the advantages offered by the DH device, it was chosen as the basis for the development.

Lens Design and Fibre Pigtail Selection

In 1975 Plessey developed a computerised numerical model ⁽⁸⁾ based on the lens geometry shown in Fig.2.3. to determine the coupling efficiency for three numerical apertures 0.16, 0.25 and 0.5. For simplicity and ease of computation the lens diameter was made equal to the fibre core diameter and the lens refractive index (n_2 of Fig.2.3) was assumed to be 1.9, which corresponds to a commonly available silica titania glass mix. The programme was expanded in subsequent years to permit independent variations to all the parameters in the system and hence complete device optimisation. This programme was used to establish the coupled power trade-offs for different fibre parameters with the aim of determining a suitable fibre pigtail.

The first step involved a collation of our previous computations and resulted in the design chart shown in Fig.2.4. which gives the maximum coupled power launchable into a particular fibre for a fully optimised, idealised (100% internal efficiency, non-absorbing and with a back reflecting contact) LED. The optimisation involves source diameter and this decides a particular maximum operating current to give a fixed maximum

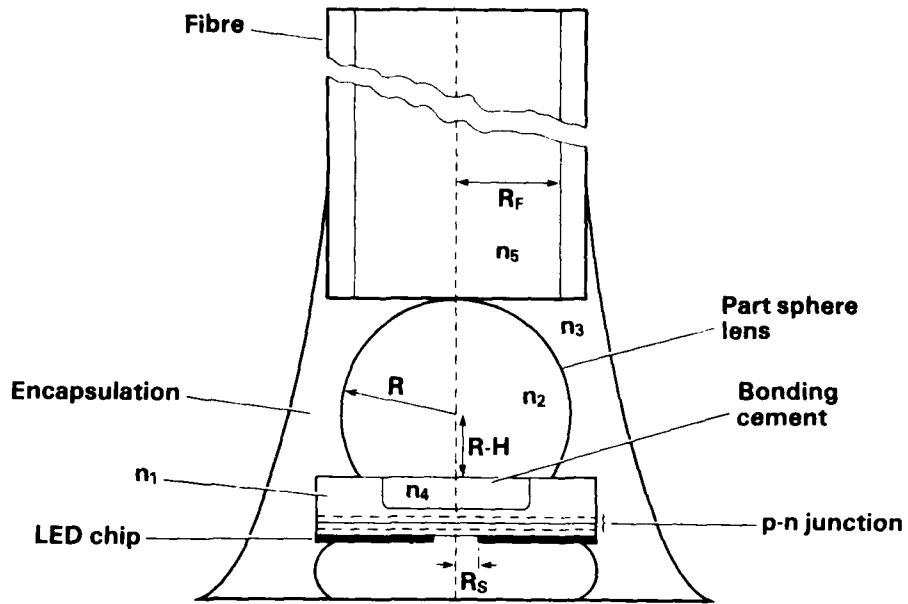


Figure 2.3

High Radiance LED Fitted with Truncated Sphere Lens

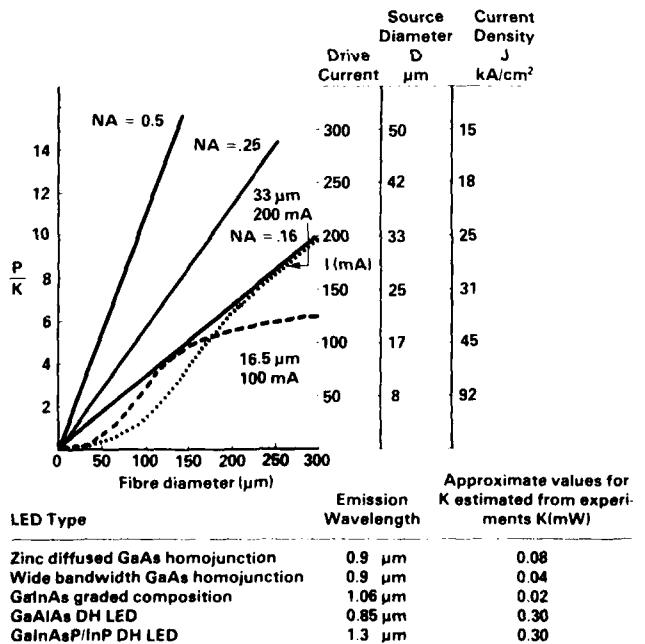


Figure 2.4

Power Coupled vs. Fibre Size for Optimum Diode and Lens

Geometry with NA as Parameter

junction temperature rise - an assumption of the model. If the device size is fixed at say 16 or 33 μm , characteristics like those shown dotted are obtained. The lines are tangents to a series of such curves.

The power which could be coupled to fibres from real LED's can be estimated from this graph if values of K , the effective internal efficiency, are estimated for the different types of LED. The table included in Fig.2.4. shows conservative estimates for K for different LED types, showing that for example 1.8mW should be launched into 100 μm 0.25 NA fibre at $\sim 120\text{mA}$ drive. Fibres which we considered are listed in Table 2.1, together with the optimum coupling computed for a 25 μm diameter source. A 25 μm source was chosen because 150mA is a reasonable maximum working current for most applications and this is the smallest source size which can operate at this current. The maximum coupling efficiency is shown in Fig.2.5 for each of the chosen fibres. We also calculated the effect of a variation in the numerical aperture of the fibre (shown dotted) assuming that the lens and diode geometry are maintained for optimum coupling to the specified NA. Clearly the launch power increases with NA and core diameter, but other factors must also be taken into consideration in the selection of the fibre pigtail, i.e. radiation hardness, handling, availability, attenuation, cost etc. Two fibres were recommended, namely the Galileo and the Corning from launch power, radiation hardness and size considerations, but the availability of the Corning 100 μm 0.3 NA fibre made this the ultimate preference.

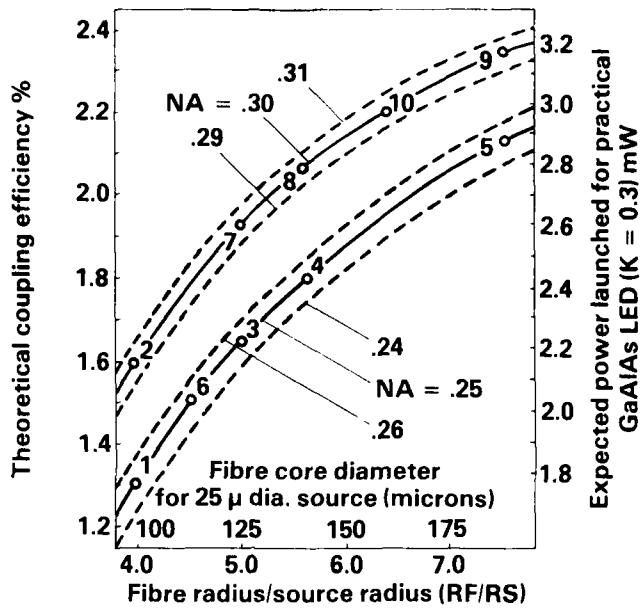


Figure 2.5

Coupled Power for 25μ Diameter Source
at 150mA Drive Current and Optimised Lens Parameters

TABLE 2.1

FIBRE DATA AND OPTIMISED LENS DATA

No.	Type	Cladding dia. (um)	Core dia. (um)	NA	Coupling efficiency %
1	ITT	140	100	.25	1.31
2	Corning	147	100	.30	1.60
3	Galileo	200	125	.25	1.65
4	Galileo	200	140	.25	1.79
5	Pilkington	245	188	.25	2.13
6	Pilkington	147	113	.25	1.51
7	#		125	.30	1.93
8	#		140	.30	2.07
9	#		188	.30	2.34
10	#		160	.30	2.20

Items 7, 8, 9 and 10 are fictitious fibres invented to show results for NA = .30

3. MATERIALS, PREPARATION AND CHARACTERISATION

A schematic of the double heterojunction structure typically used in high radiance LED structures is shown in Fig. 3.1. Here the active layer of GaAlAs is sandwiched between two higher bandgap layers, also of GaAlAs, and is normally doped p-type and has a thickness of $\sim 1\mu\text{m}$. This sandwich structure is supported by an n-type GaAs substrate and is overlaid with a thin p^+ GaAs layer for ease of contacting. The multilayer structure is grown epitaxially onto the GaAs substrate by Liquid Phase Epitaxy (LPE).

The LPE equipment is illustrated in Fig.3.2. This shows the graphite slider assembly containing the GaAs substrate in a recessed baseplate and a series of melts contained in a multi-pot crucible. The melt constituents are selected to suit the designed layer structure, with metallic gallium as the solvent, arsenic and aluminium as the solutes, and germanium and tin as the p-type and n-type dopants. Fig. 3.3. is a photograph of the graphite slider. A feature here is the pre-growth slice which serves to precisely equilibriate each melt immediately prior to epitaxy.

The graphite slider, complete with melts and substrates, is loaded into the furnace system, shown schematically in Fig.3.4. Features of this system are:-

- a) pure hydrogen atmosphere
- b) UHV and mass spec. system for determination of oxygen and water - very important when growing aluminium containing compounds.⁽⁹⁾
- c) nitrogen flushed loading bay to exclude oxygen from the system.
- d) roll-off furnace for ease of loading and rapid turn round.

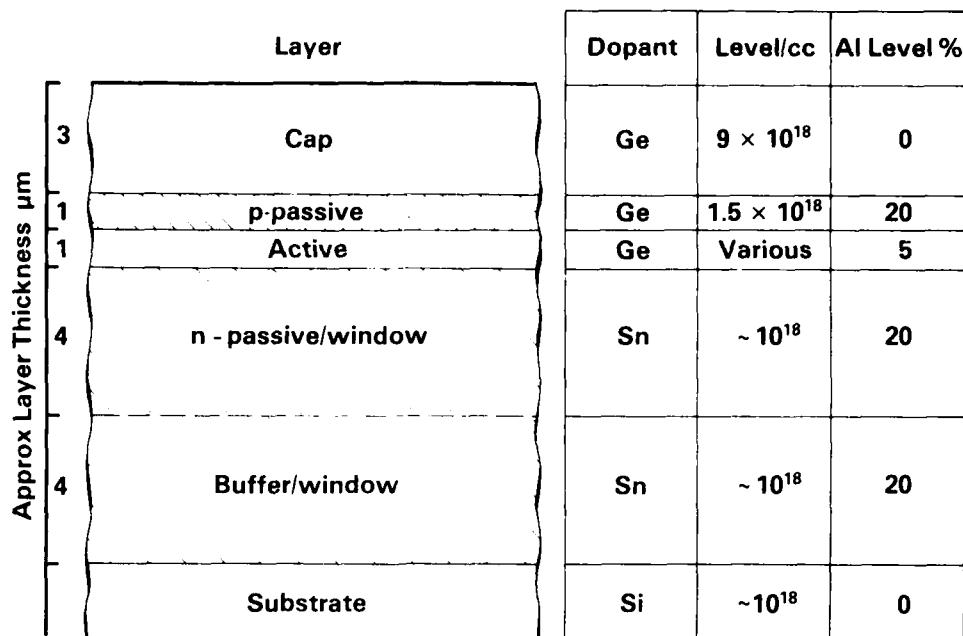


Figure 3.1

GaAs/GaAlAs Double Heterostructure Schematic

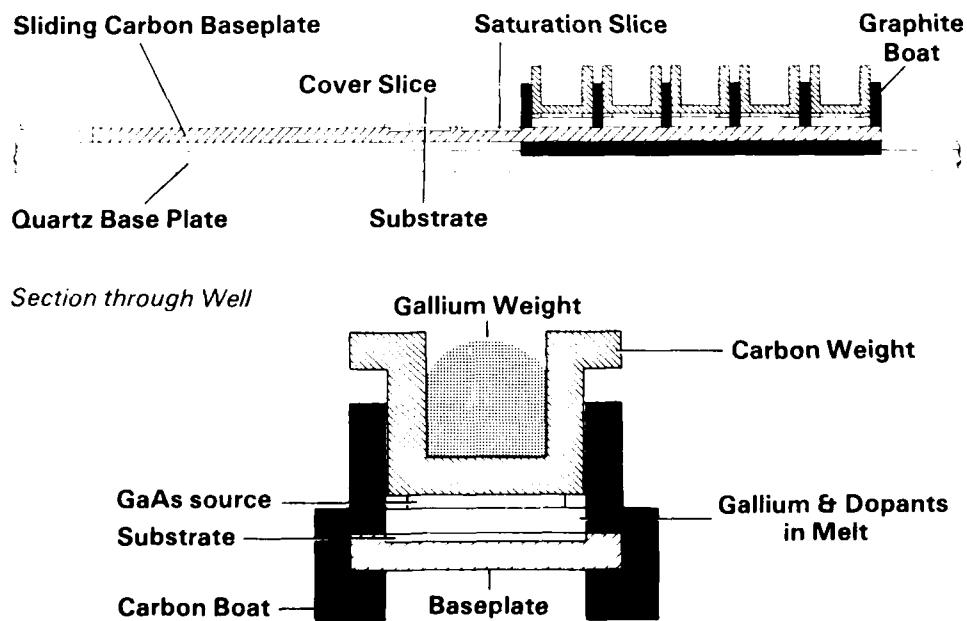


Figure 3.2

Liquid Phase Epitaxy (Graphite Boat & Sliding Baseplate)

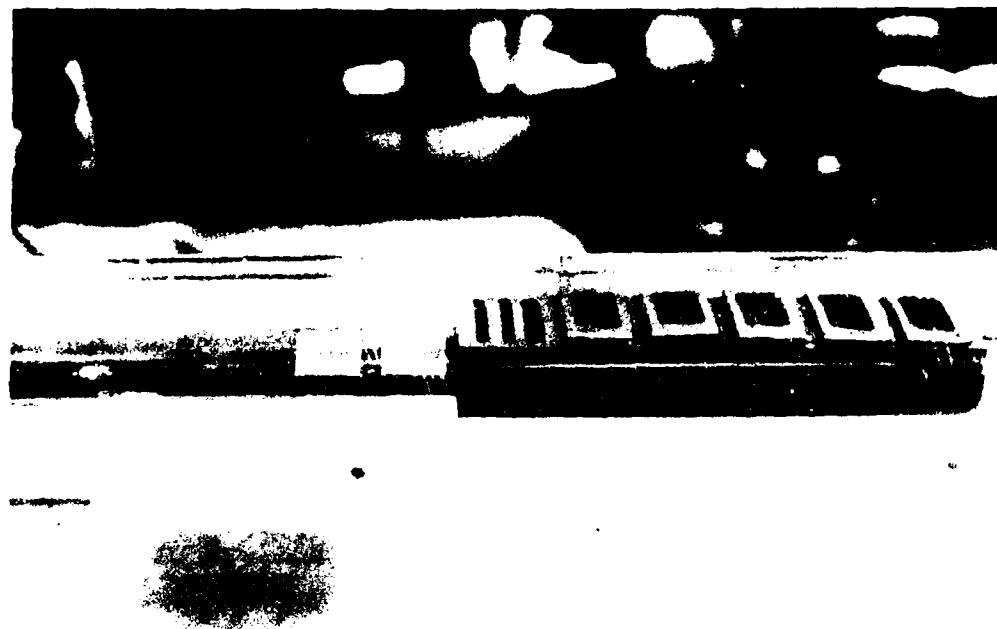


Figure 3.3
Photograph of Graphite Boat and Slider

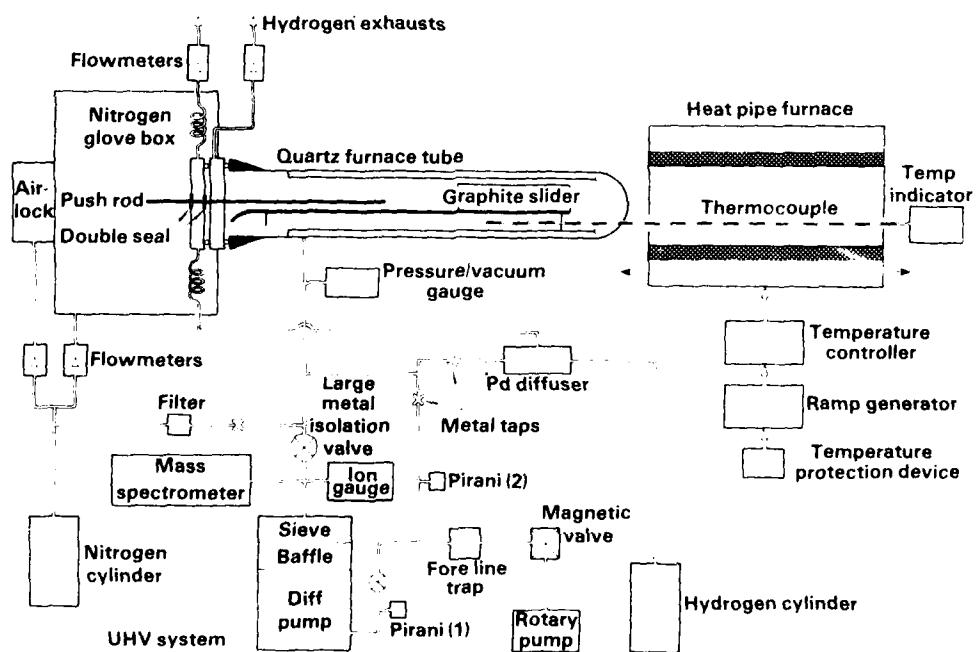


Figure 3.4

L.P.E. System with U.H.V. and Mass Spectrometer Attachments

The pre-growth and growth sequence includes hydrogen and vacuum bake-outs and leak-tightness of the system is checked by establishing an ultimate vacuum of $\sim 1.5 \cdot 10^{-8}$ T and H_2O level of < 0.5 ppm.

Growth temperature is 810^0C ramping down at $-0.3^0C/min$. Growth of each layer is initiated by movement of the substrate containing baseplate, actuated by a quartz push-rod through a double seal.

The good quality of multiple layers grown in this system is indicated by the macrograph shown in Fig. 3.5., which also shows a cleave and stain micrograph of a typical structure.

The properties of the central active layer largely determine the device performance characteristics. In the present programme we have adjusted the active layer parameters in order to establish the required device performance.

This was achieved in the series of layers P93, P111, P112 and P122, whose active layer parameters are detailed in Table 3.1. (page 18). From the performance of devices fabricated from these layers, detailed later, we established an optimum layer structure to meet the required specification in terms of speed and coupled power. Three multilayer structures were then grown to this specification for subsequent device fabrication and characterisation. These were P124, P135 and P141; their active layer doping levels and thicknesses are also given in the Table.

The characterisation of thin multi-layer structures presents some special problems. Detailed characterisation by X-ray and electron microscope techniques is carried out (10), but is too time consuming for routine use. A contact resistance profiling method (11) however, has been developed which gives rapid semi-quantitative information on layer thickness, doping levels and composition within thin multi-layer structures. The technique is

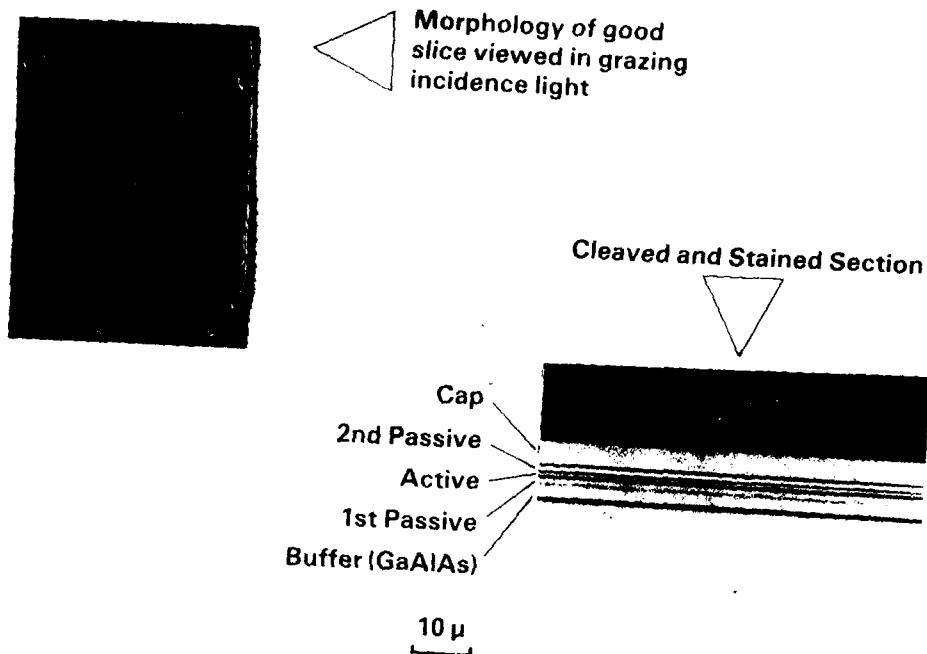


Figure 3.5
Morphology and Cross Section of LPE Wafer

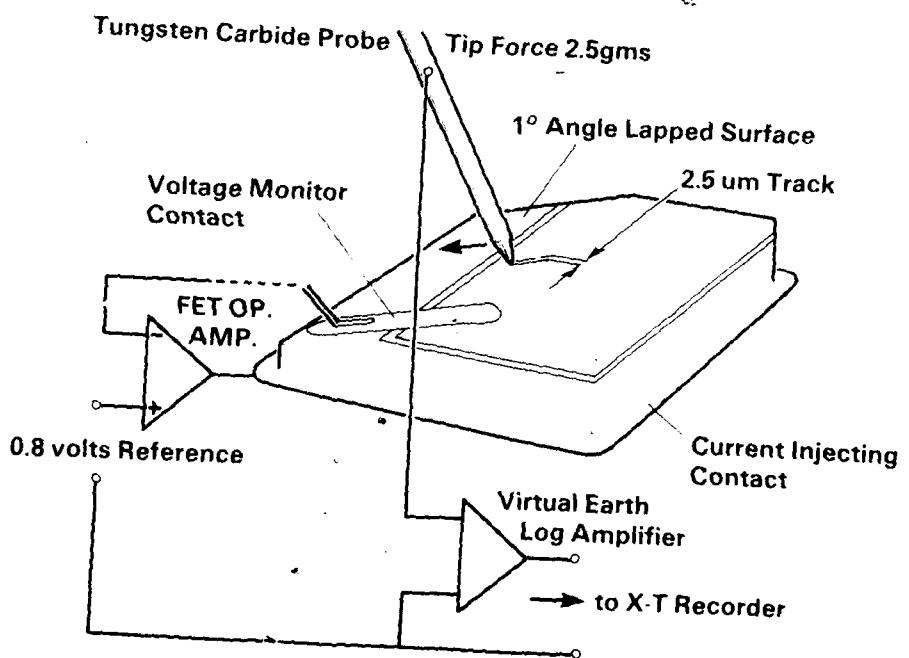


Figure 3.6

Contact Resistance Profiler
-16-

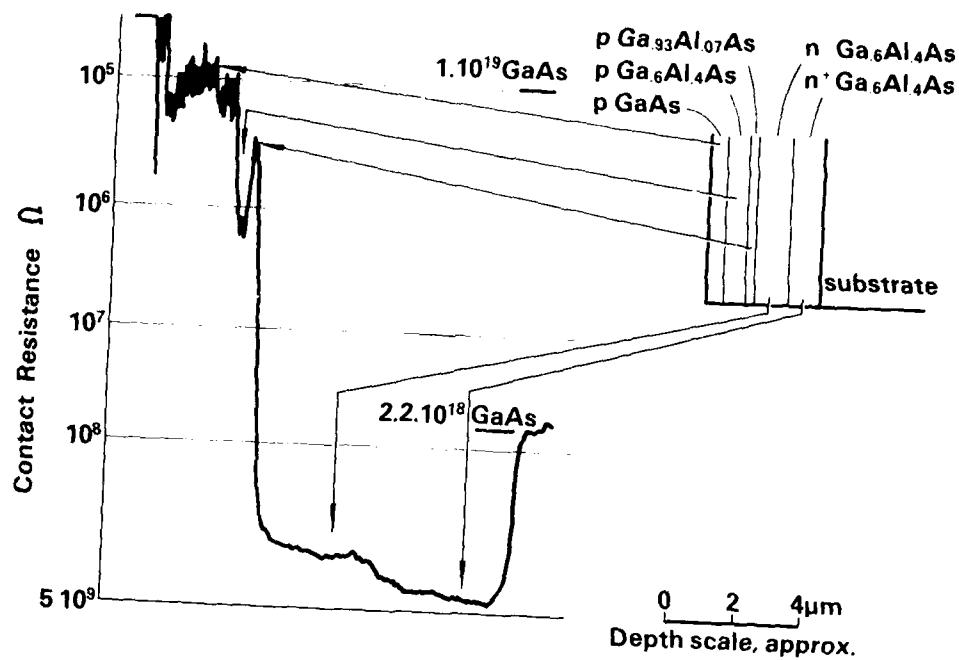


Figure 3.7
GaAlAs DH Multilayer Profile

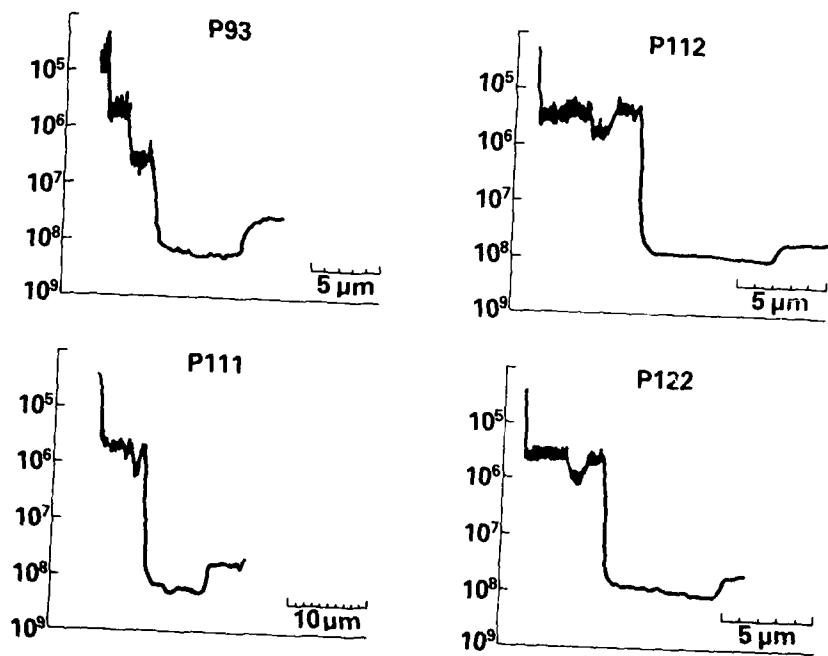


Figure 3.8
Contact Resistance Profiles

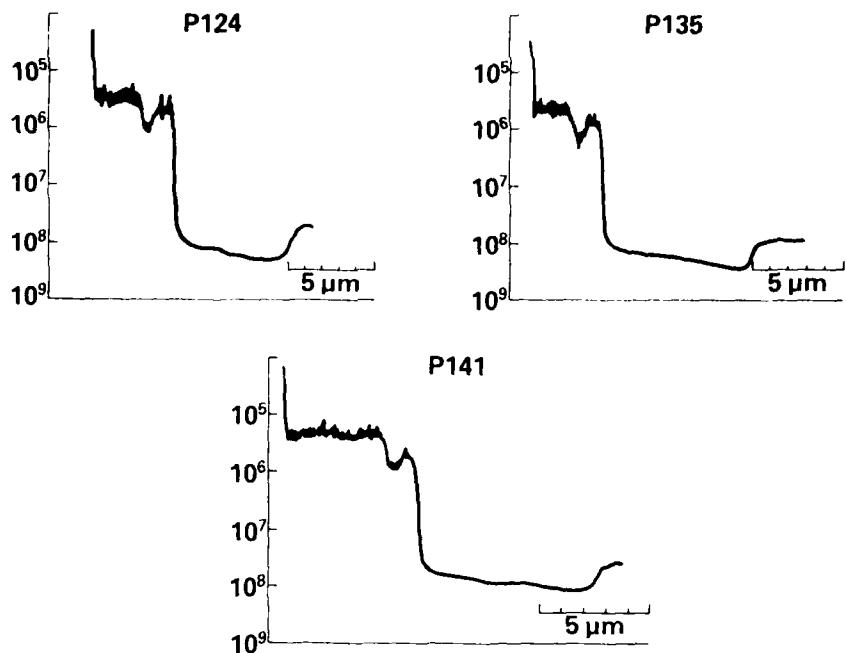


Figure 3.9

Contact Resistance Profiles

TABLE 3.1

ACTIVE LAYER DETAILS

Layer No.	Active Layer Thickness	Ge in melt mgms/g Ga	Doping Level
P93	1.2 μm	10	2×10^{18}
P111	1	40	6
P112	1.8	40	6
P122	1.3	25	4.5
P124	1.25	25	4.5
P135	1	25	4.5
P141	0.8	25	4.5

illustrated in Fig. 3.6, where it is seen that the sample is firstly bevelled then tracked with a light probe whilst monitoring the resistance between the probe and the sample. A plot of this resistance, combined with calibration data, as a function of depth in the sample, yields data at high spatial resolution on the carrier concentration/composition profile. An example of such a plot and its relationship to the multi-layer structure is shown in Fig.3.7. Profiles prepared in this manner are shown in Fig.3.8. for the optimisation series P93, P111, P112 and P122, and in Fig.3.9. for the final device layers P124, P135 and P141.

4. DEVICE FABRICATION

In this section we deal with device fabrication, from wafer processing through to pigtailing the completed device.

Fig.4.1.(a) shows the diode structure in cross section with the layer structure detailed. The departure from the more conventional square structure to a 10x14 mil. shape allows us to include a large, well supported area for bonding in a die accommodating a relatively large micro-lens. The perspective view indicates the relative sizes of lens and die (Fig.4.1.(b)).

The diode processing sequence is shown schematically in Fig.4.2.(a) through (h). We start with a slice cleaved from an LPE wafer with a thickness of around 160 - 180 μ m. The p-side is metallised and has small dots of gold plated on to form proton shields (b). Proton bombardment follows and the beam energy is selected to provide a semi-insulating layer in non-contact areas which extends to just short of the active layer (c). The slice is then thinned from the n-substrate side to about 60 μ m total thickness and the n-side metallisation

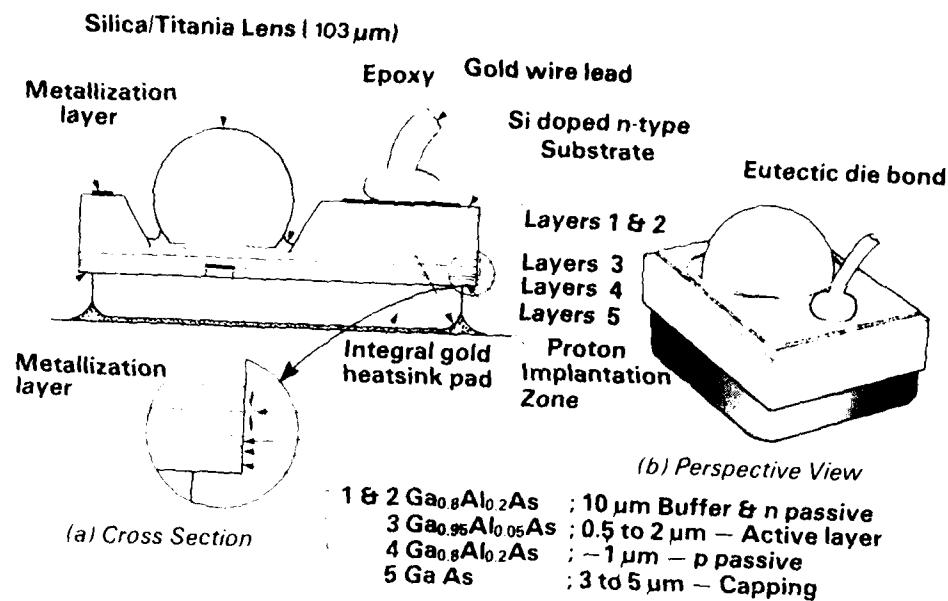


Figure 4.1

Die and Lens Layout 10 x 14 Mil Offset Well

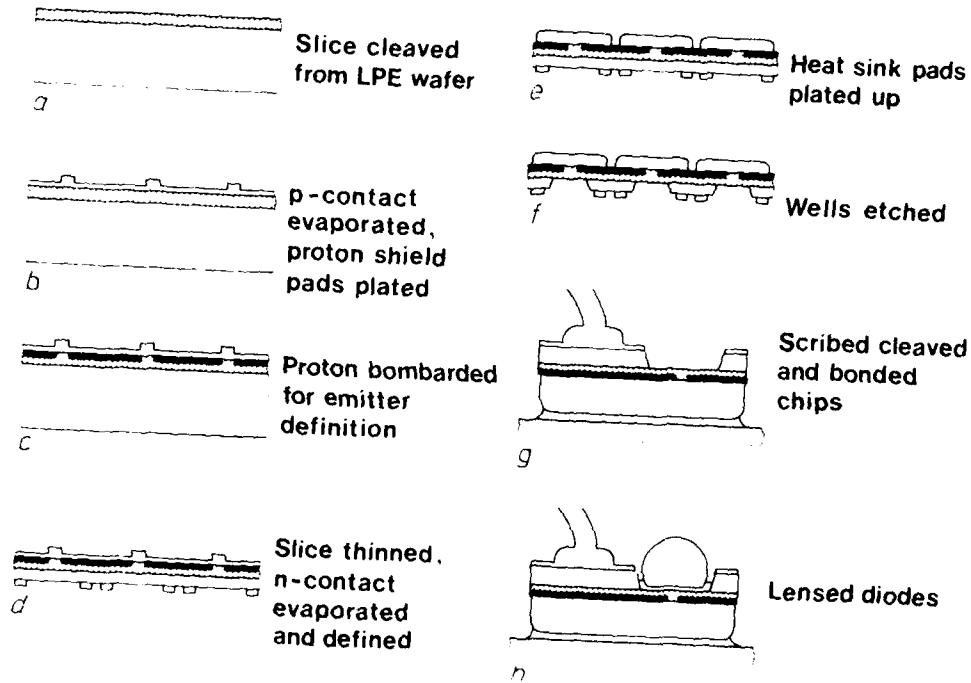


Figure 4.2

Schematic Outline of LED Fabrication

applied and defined (d). Gold heat sink pads are then plated on the p-side to give a low thermal impedance structure (e). Returning to the n-side, wells are etched into the GaAs substrate using a selective etch which stops at the GaAlAs boundary of the first buffer layer (f). The slices are then scribed and cleaved into dice, which are now shown in the long section (g). These are eutectic bonded to S4 packages and the n-side contacted to the package flange using a pulse tip gold wire bonding method. Finally, lenses are epoxy bonded in the wells (h). Figs. 4.3. through 4.7. illustrate some of these processing stages. Fig. 4.3. shows a cleaved and stained cross section of a wafer after proton implantation - the gold proton shield and the semi-insulating layers can be seen quite clearly.

Fig.4.4. is a scanning electron micrograph (SEM) section of an implanted diode and the lower figures show the wells - note the plane surface of the well base. The selectivity of the well etch and the planarity of the well base can be clearly seen in Fig.4.5. which is a SEM of a cleaved and stained section of a completed chip with the heat sink pad removed. The material above the emitting area is GaAlAs which is virtually non-absorbent to the emitted light.

The titania-silica (TS) lenses are prepared from TS spheres. The spheres are first selected for diameter by sieving and are then ground down to the correct truncation. Fig.4.6. shows the flat surface of this truncation and some lenses in various attitudes from which their cross section can be seen. Fig.4.7. is a SEM micrograph of the bonded device complete with the titania-silica microlens attached.

The schematic view of the pigtailed device structure in Fig.4.8. indicates how the final assembly of the device is accomplished. It shows the LED chip complete with lens bonded to the S4 package, which consists of a copper stud,

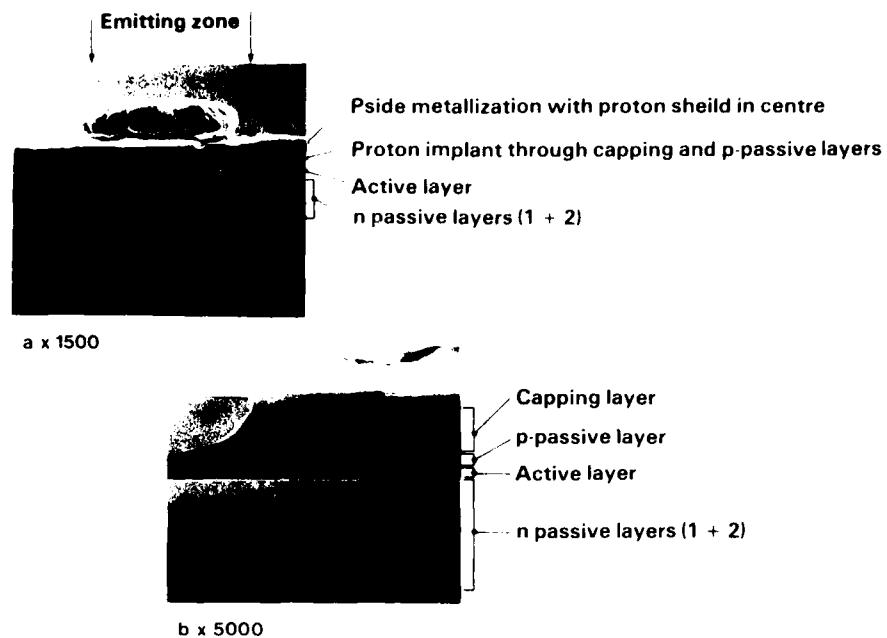
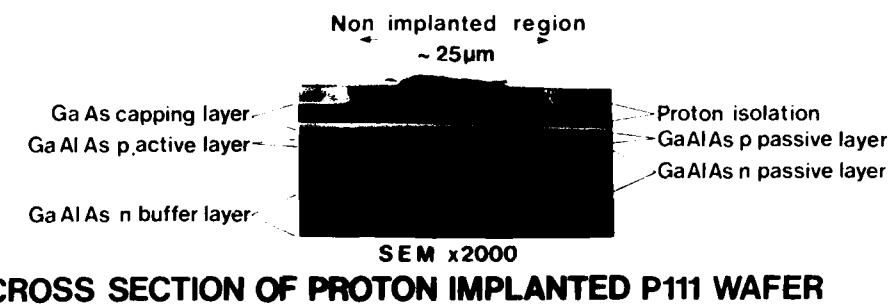


Figure 4.3

P122B Process Slice after Proton Implant Cleaved and Etched Section



CROSS SECTION OF PROTON IMPLANTED P111 WAFER



Figure 4.4

Photomicrographs of P111 Wafer N Side Showing Wells in Offset Geometry

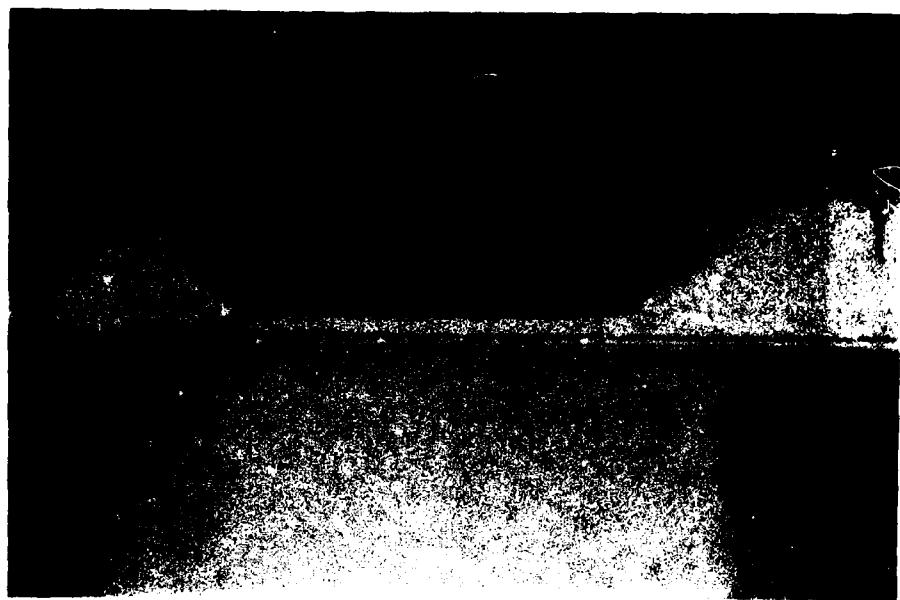


Figure 4.5
LED Cleaved Cross-Section

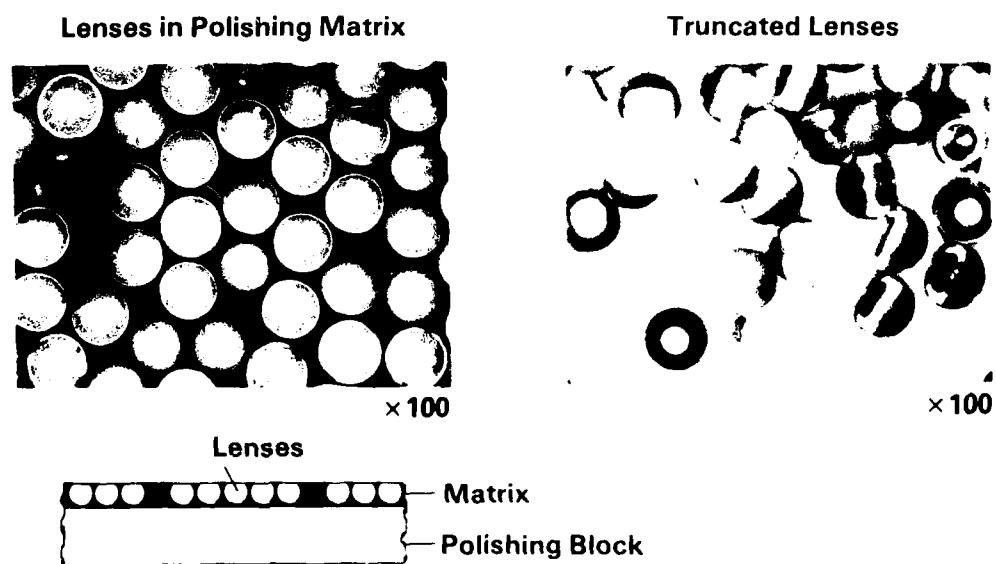


Figure 4.6

Lens Truncation



Figure 4.7

SEM Micrograph of Bonded, Lensed Device

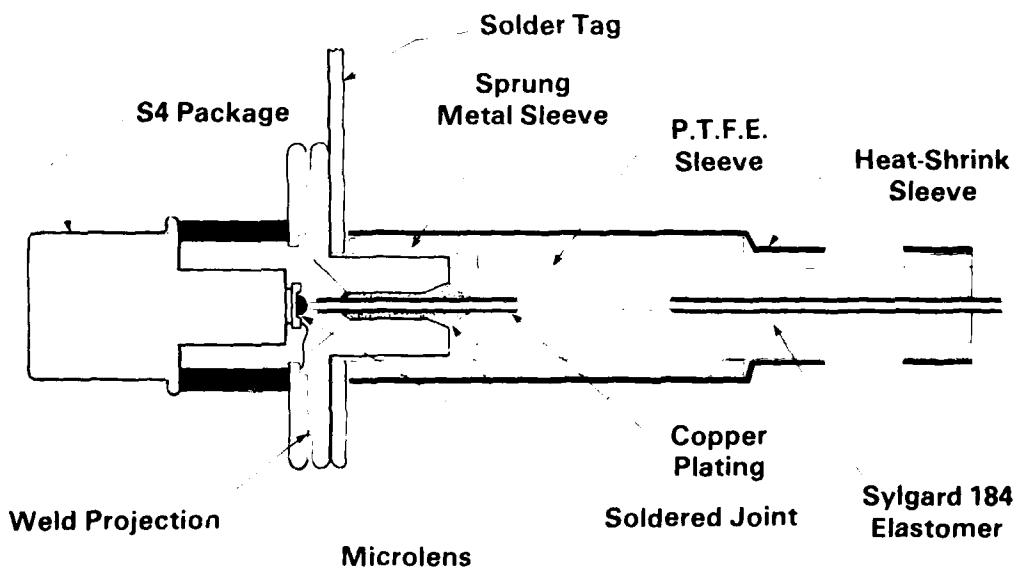


Figure 4.8

Pigtailed Device - Schematic

ceramic insulator and Kovar or copper-Kovar flange. The stud and flange are gold plated. The first seal after lensing is the top cap weld. The top cap is of gold plated Kovar and is a standard component modified with a $700\mu\text{m}$ (28mil) diameter hole drilled through and chamfered both ends. The top chamfer acts as a solder reservoir to give increased solder to fibre contact area and the lower chamfer, which is made after gold plating to reveal the Kovar, inhibits solder flow into the chip zone. A soldering tag is welded onto the device at this stage. The second seal is made by soldering a prepared fibre into the top cap. Finally the fibre support system is added for stress relief between the rigid solder support and the fully flexible fibre. This is made up of sprung metal housing holding a PTFE sleeve filled with silicone elastomer and the assembly is sheathed with heat shrinkable sleeving.

Fibres are prepared by stripping back the cladding and metallising the surface using a proprietary process. Copper is then plated on to this metallisation, to a thickness providing a loose fit in the top cap. These two stages are shown in Fig. 4.9.

The fibre is then aligned through the device top cap and soldered into position. Alignment is accomplished by monitoring the optical power output from the pigtail during the soldering operation. The appearance of the device at this stage is shown in Fig.4.10 where the solder joint and metallisation can be seen.

Fig.4.11. shows the pigtailed device complete with sheathing and mounted in a standard heat sink clamp, and Fig.4.12. gives the outline and major dimensions.

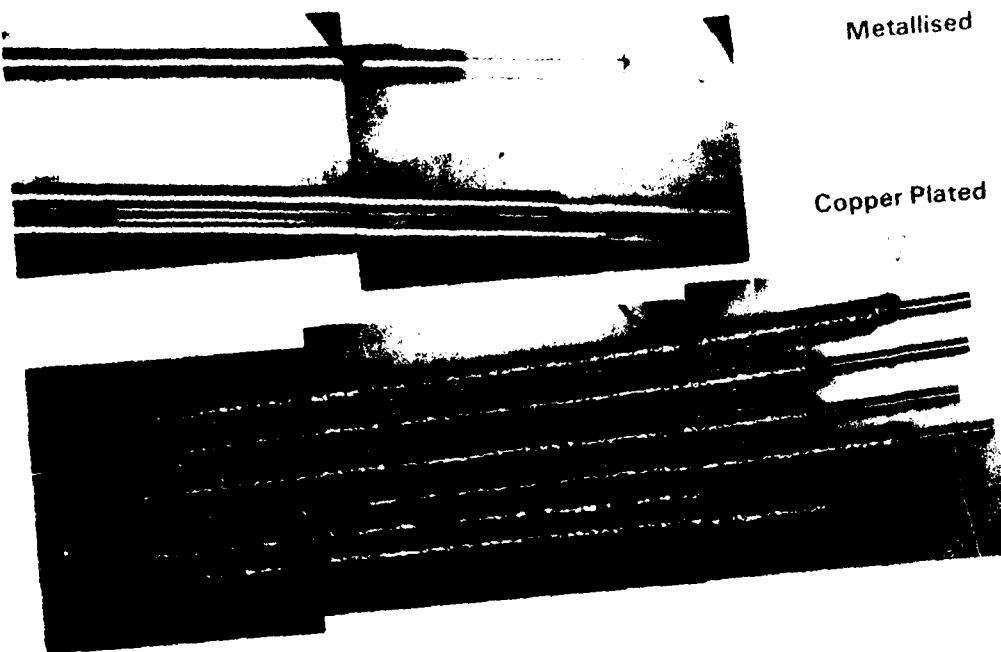


Figure 4.9
Fibre Metallisation



Figure 4.10
photograph of Soldered-in fibre

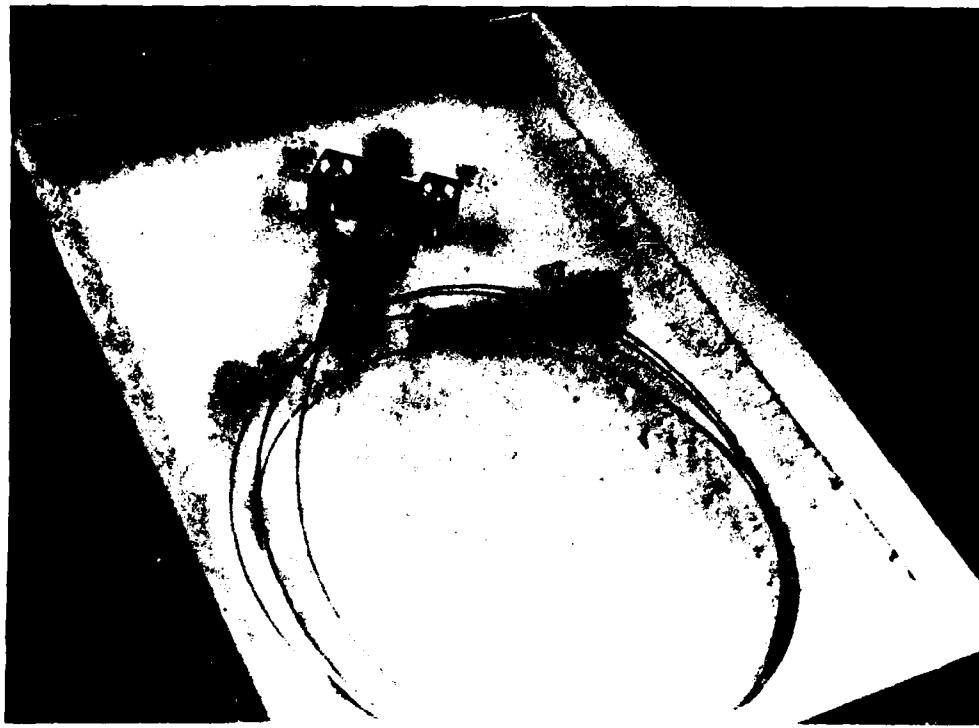


Figure 4.11
Photograph of Device Ready for Despatch

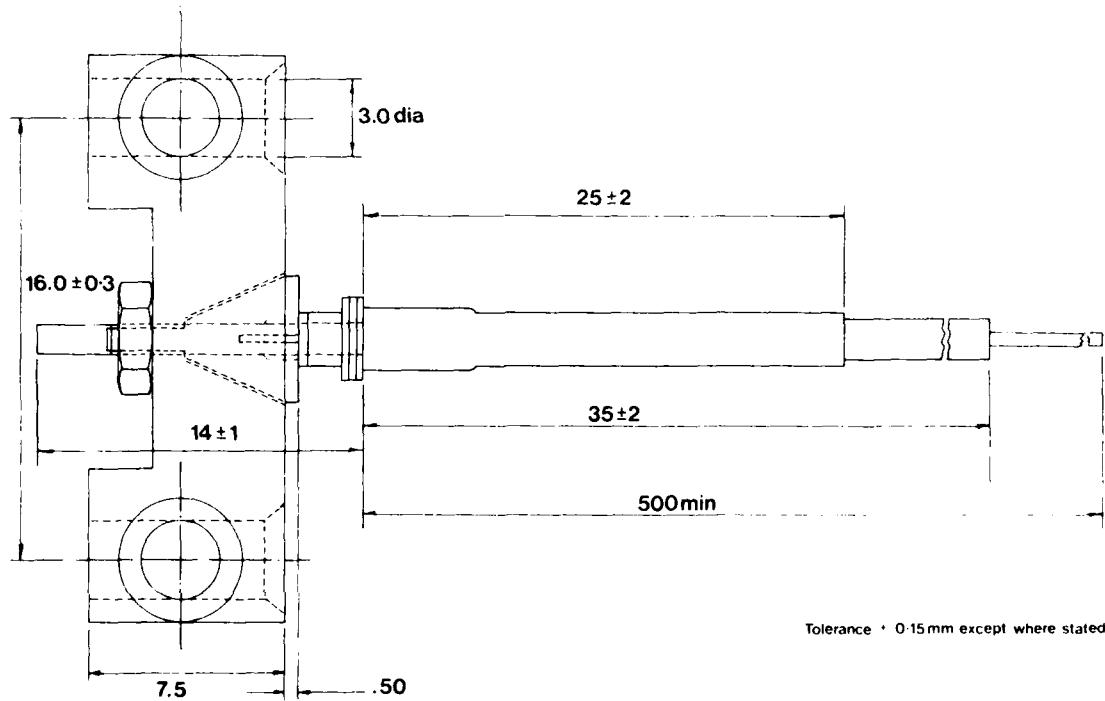


Figure 4.12

Outline of Pigtailed LED in Clamp giving Overall Dimensions

5. TEST PLAN DEVELOPMENT

Fig.5.1. shows an outline of the testing scheme. This scheme includes characterisation and screening tests and also resolution of uncertainties.

The characterisation testing was designed to measure the parameters of the device which would be required for a formal specification in keeping with MIL-S-19500F. The provisional screening test was designed to be equivalent to conventional production and quality control testing of high quality MIL-Spec LED's. The uncertainties, p-n junction optimisation, pigtail hermeticity and the effects of mechanical shock appear as loops and branches in the testing scheme. These will be dealt with in detail in Sections 6, 7 and 8, pages 23 and 32. The tests made at the diode stage are included to ensure that defective devices are not carried through to the later more demanding fabrication stages.

The test plan that was developed and used for this effort is entitled 'Environmental Test Plans/Procedures' and is included in this report as Appendix A.

Characterisation testing is detailed in Section 9, Life-tests in Section 10 and Screening tests in Section 11.

6. SPEED/RADIANCE OPTIMISATION

An initial set of experiments was carried out to establish the speed/power trade off by deliberately varying the doping level and the thickness of the active region of the device. Four layers P93, 111, 112 and 122 were used in this experiment and the properties of these layers are listed in Table 6.1. In general, higher doping levels lead to increased speed but decreased power. The active layer is Ge doped and the doping level is controlled by the percentage of Ge present in the melt during growth. The doping level was varied from 2×10^{18} to $5 \times 10^{18} \text{ cm}^{-3}$ and the

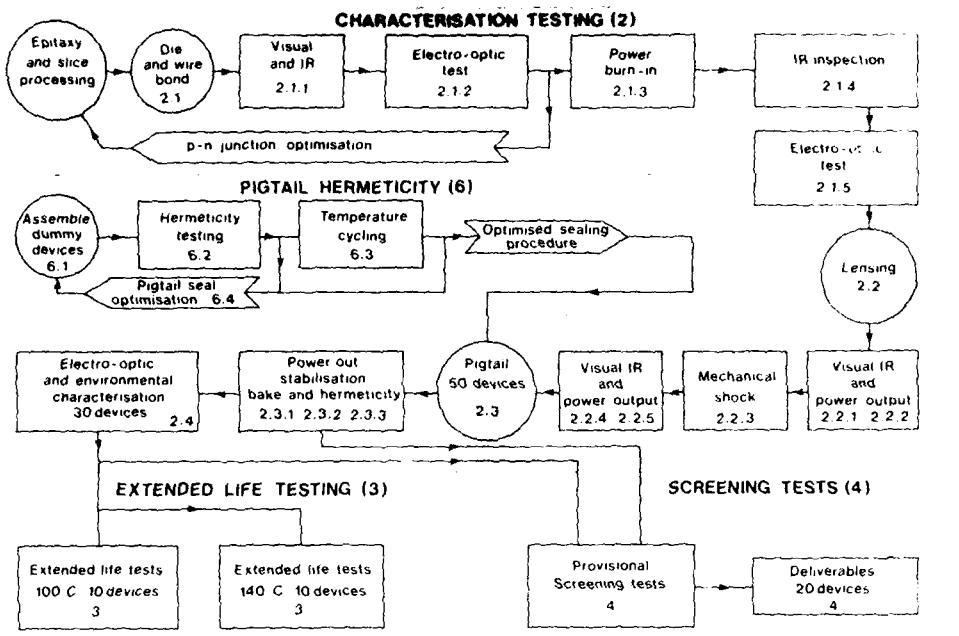


Figure 5.1

Outline of Testing Schedule

TABLE 6.1

SUMMARY OF DEVICE DATA

LPE WAFER NUMBER	ACTIVE LAYER, Ge DOPED			PULSE RESPONSE		RADIANCE W/st/cm ²	RELATIVE RADIANT INTENSITY (Arbitrary units)	WAVELENGTH	
	Melt Addition Level mgGe/gm melt	Thickness μm	Proton Isolation Active Area Diameter μm	t _r nS	t _f nS			λ _p nm	Δλ nm
P93A	10	1.5	oxide isolation (20)	30	7.8	122	-	850	49
P93	10	1.5	27	5.6	7.6	93	0.9	850	49
P111	40	1.0	25	2.6	3.6	85	0.8	866	50
P112	40	2.1	25	4.2	5.0	83	0.92	872	56
P122	25	1.2	21	2.6	3.8	100	1.0	874	54

thickness from 1.0 microns to 2.1 microns. These layers were then processed into high radiance LED structures and measurements were carried out on both efficiency (or radiance) and speed of response as detailed in Table 6.1. In general, all four layers provided adequately high values of radiance and so subsequent tailoring of the layer parameters was aimed at the speed requirement. The results are given in Fig.6.1. which shows plots of rise time and fall time versus the doping level in the active layer expressed as percentage of dopant in the melt. The specified requirement and goal of 6n sec and 3n sec respectively are shown on the vertical axis. The results on P111 and P112 show the effect of active layer thickness - thin active layers leading to lower rise and fall times.

Plotting half power bandwidths versus drive current in Fig.6.2. shows that at lower than maximum drive currents the bandwidth falls off and that the 25mg/g melt addition level would fulfil the 100 MHz requirement over most drive conditions. The oxide isolated devices (P93A) are much slower than proton bombardment isolated diodes and this is also indicated by t_r , t_f values of 30ns and 20ns respectively. The dependance of bandwidth on the square root of the bias current indicated by Fig.6.2. is characteristic of a plasma density dependant recombination time.

Clearly the best designs are P111 and P112 both of which meet the requirement and approach the goal of 3n sec. However P112 is preferred since it is slightly less heavily doped and consequently provides somewhat higher power capability.

Based on these results, three device structures were then grown in which the active region had a doping level of $4.5 \times 10^{18} \text{ cm}^{-3}$ and thickness of 0.8 - 1.25 microns as listed earlier in Table 3.1. These wafers were used in the fabrication of the devices for full characterisation including the

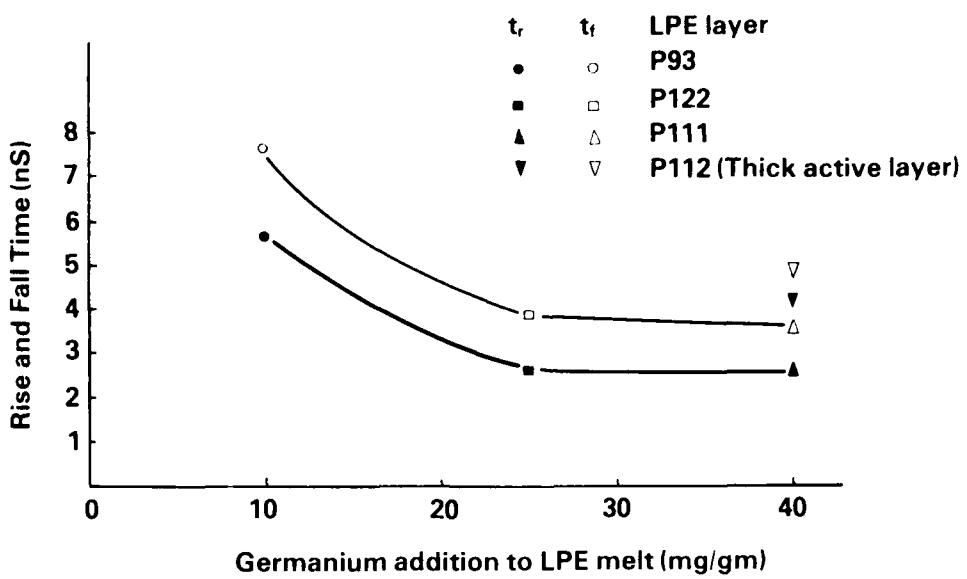


Figure 6.1

Device Rise and Fall Times as a Function of Active Layer Doping

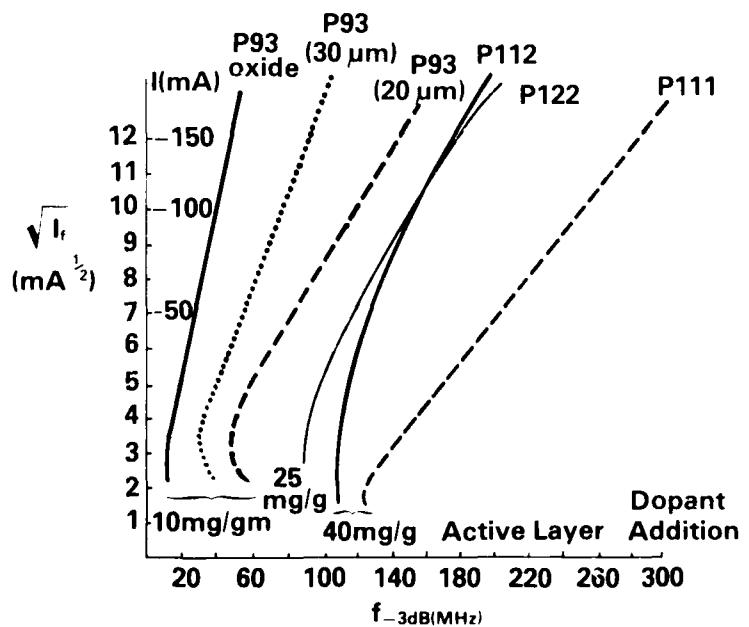


Figure 6.2

Half Power Bandwidth Vs $\sqrt{\text{Drive Current}}$

deliverables. The wafers here were P124, P135 and P141, and the fabrication steps were as outlined in section 4 of this report.

7. SHOCK TESTING OF LENSED DIODES

Another question that required early attention during the programme was the strength of the epoxy bond attaching the lens to the diode chip.

In order to test this, lensed diodes were subjected to 50G, 11msec and 100G, 6msec shocks, axially and radially and at 25 and 125°C, in accordance with MIL-STD-202E, method 213B.

The axial shock pulse direction was chosen so as to place the lens-chip bond in tension. The shock testing jig which was constructed to fit on the top of a standard shock testing mounting cube for axial and on the side of the cube for radial shock is shown in Fig.7.1. Also shown is a thermocouple clamped to one of the LED packages which was used for monitoring the diode temperature.

Table 7.1. shows the complete sequence of testing here and it can be seen that no observable damage resulted from the range of shock conditions applied. Power out values as determined into a free fibre showed only minor changes which could be due to fibre alignment and/or systematic equipment errors. This is therefore considered as a completely successful test sequence and shows clearly that we have a mechanically rugged lens-die attachment technique.

8. HERMETICITY

Hermeticity of the pigtail structure is one of the key requirements for this device. Preliminary work fell into two areas on this programme; yield improvement and testing the device complete with fibre pigtail to demonstrate hermeticity.

Table 8.1. summarises tests made on dummy devices i.e. mechanical assemblies without working dice to establish the best

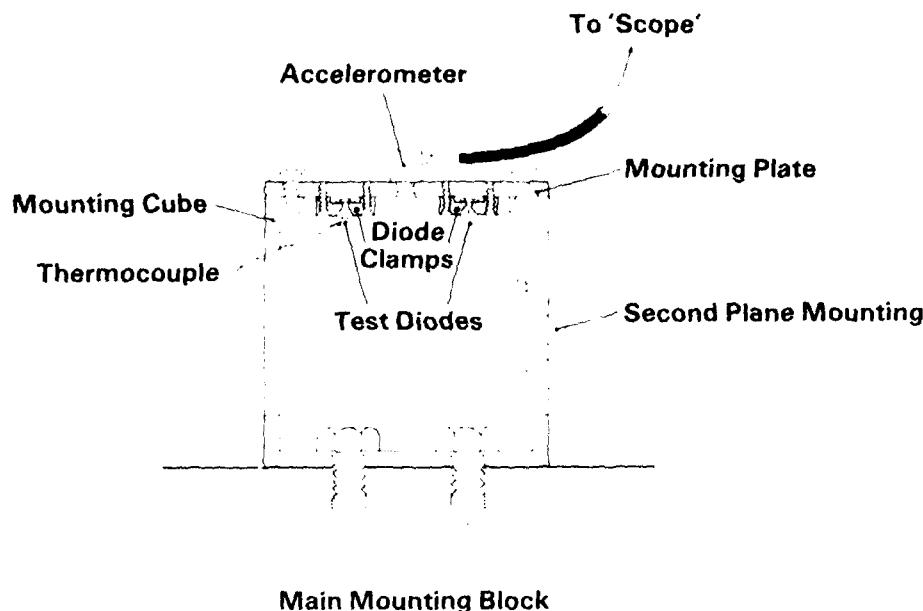


Figure 7.1

Mechanical Shock Test Mounts

TABLE 7.1

SHOCK TESTING RESULTS

Device No.	Power into Free fibre (uW)	Inspection Results				Power into Free fibre (uW)	Inspection Results				FINAL Power into Free fibre (uW)
		After 50G Shock (11ms)		After 100G Shock (6ms)							
		25 C AXIAL	25 C RADIAL	125 C AXIAL	125 C RADIAL		25 C AXIAL	25 C RADIAL	125 C AXIAL	125 C RADIAL	
31	418	✓	✓	✓	✓	399	✓	✓	✓	✓	418
32	627	✓	✓	✓	✓	646	✓	✓	✓	✓	608
34	608	✓	✓	✓	✓	608	✓	✓	✓	✓	589
35	456	✓	✓	✓	✓	456	✓	✓	✓	✓	437
36	760	NT	NT	NT	NT	NT	NT	NT	NT	NT	222
37	684	✓	✓	✓	✓	646	✓	✓	✓	✓	570
39	532	✓	✓	✓	✓	532	✓	✓	✓	✓	513
40	684	✓	✓	✓	✓	684	✓	✓	✓	✓	608
41	646	✓	✓	✓	✓	608	✓	✓	✓	✓	570
42	608	✓	✓	✓	✓	570	✓	✓	✓	✓	608
44	760	✓	✓	✓	✓	760	✓	✓	✓	✓	722
47	760	NT	NT	NT	NT	NT	NT	NT	NT	NT	760

✓ indicates inspection pass. Failed to pass inspection
 * indicates pass at above test level but failed at next level

conditions for welding and fibre sealing. The test devices were of two types; solid top caps to establish flange weld conditions and stub fibre devices without cladding to provide information on the fibre solder process. The site of gross leaks is also recorded in Table 3.1. The pigtailed devices which gave no leak indications were submitted to thermal shock, initially 5 cycles of 30 minutes at -55°C followed by 30 minutes at $+85^{\circ}\text{C}$ and then 5 cycles of 30 minutes at -65°C followed by 30 minutes at $+125^{\circ}\text{C}$. The devices were leak tested after each shock condition.

A number of different welder power supplies and conditions were evaluated and, as can be seen in Table 3.1, a satisfactory yield of hermetically sealed dummy devices which withstood thermal shock tests was eventually achieved. These were obtained using a high-power supply and inert gas atmosphere for the weld, with pre-tinned top caps for the fibre seal. A further yield improvement resulted from a change to a package with a copper Kovar bimetallic flange which reduced the number of ceramic to flange failures.

Hermeticity testing of the completed pigtailed devices was complicated by absorption and desorption on the fibre cladding materials. Fig.8.1. shows the results of absorption/desorption tests on Corning S.D.F. and Galileo Gallite 5020 clad fibres. It can be seen that with the selected fibre (Corning S.D.F.) sufficient desorption has taken place in the first twenty minutes to permit detection of fine leaks. This period is within the allowed dwell time of 30 minutes (MIL-STD 750B 1017).

A further difficulty was experienced in testing for gross leaks. If the test was made after sheathing, spurious type 2 (medium size) leaks were observed (i.e. gas bubbles from the plastic support encapsulation). For this reason hermeticity tests related to characterisation of pigtailed devices were made immediately after the fibre soldering step. A disadvantage

TABLE 8.1

PIGTAIL HERMETICITY TEST

W - Leak at Weld C - Leak at Ceramic/Flange Joint S - Leak at Solder Seal	Solid Caps			Pigtail Devices			Temp. Cycle 55 + 85°C x 5			Temp. Cycle 65 + 125°C x 5		
	Starts	Gross	Fine	OK	Starts	Gross	Fine	OK	Starts	Gross	Fine	OK
1KVA Welder	4 3 3 3	3 3 1 2	0 0 0 1	1								
Weld under Forming Gas	3 3 3	1 2 0	0 1 1		3	2W	0	1				
Electrodes Aligned	4 4	1 2	1 0	4 2								
Phase master Welder 8KVA	10 3 7 6 6 5 3 6	2 0 7 6 5 5 1 0	0 3 0 0 0 0 0 5	8 0 0 0 1 0 2 1	15	0	3	1W	0 3	2 0 3 3	1W 0 0 0	1 0 0 3
Pre-Tinned Cap					12	5S	2	5	5	1W	0	4
Bi-Metal Package	10 6 8 8	0 0 0 0	0 0 8 1	10 6 8 7	1C	1	5	0	0 5	5	0	1
										15	0	2
					6	0	0	6	6	0	0	6
									6	0	0	6

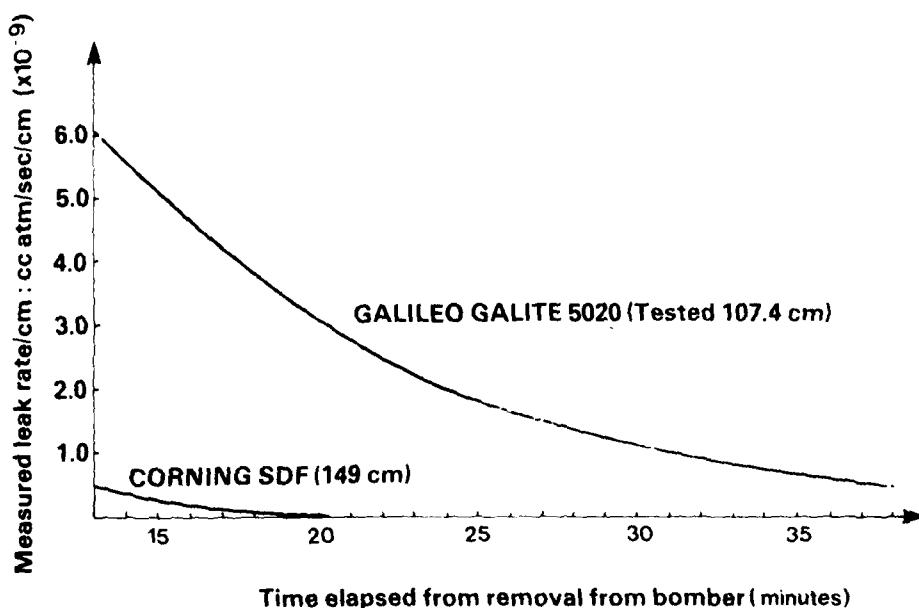


Figure 8.1

Fibre Desorption

of this procedure was the need to handle devices in a fragile state i.e. with an unsupported, uncoated fibre at the entry point to the package. Careful handling during leak testing procedures was necessary to minimise breakages.

9. CHARACTERISATION TESTING

In this section are described the test methods employed, followed (where appropriate) by the results of measurements on devices from three LPE wafers, P124, P135 and P141.

The sequence follows that of the Test Plans and Procedures Document (TPPD) of Appendix A and the figures in this section include the TPPD section numbers.

9.1. Tests on Non-Pigtailed Devices

9.1.1. Inspection

This inspection was made using a microscope fitted with a CCTV camera which enabled the bonded die to be inspected in visible and infra-red light.

The visual inspection is to ensure that dice preparation, die and wire bonding are all to sufficiently high standards and also that the base of the etched well is clear and free from excessive blemishes. The infra-red inspection is to ensure that faults such as non-uniformity of light emission and dark line defects in or near the emitting zone are eliminated at an early stage in fabrication.

9.1.2. Radiance

Radiance measurements are made before and after the power burn-in detailed in section 9.1.6. Fig.9.1. shows schematically the method of measurement, which is included within the optics of the CCTV inspection system. The measured data is reduced to a cumulative

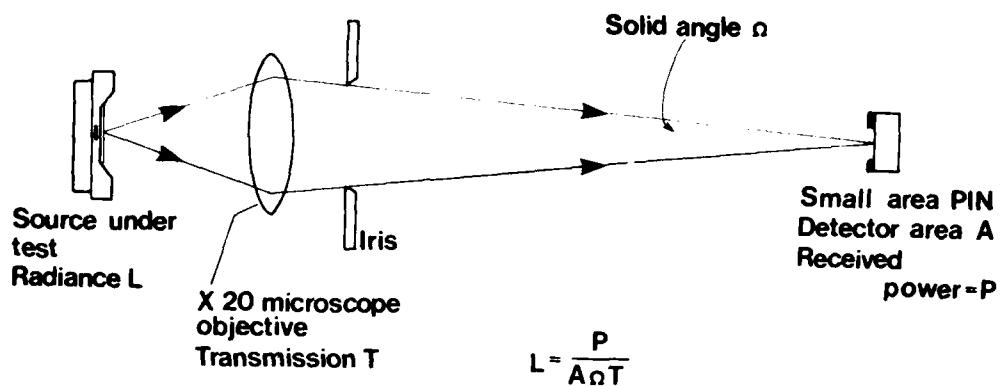


Figure 9.1
Radiance Measurement (L) (TPPD 5.2)

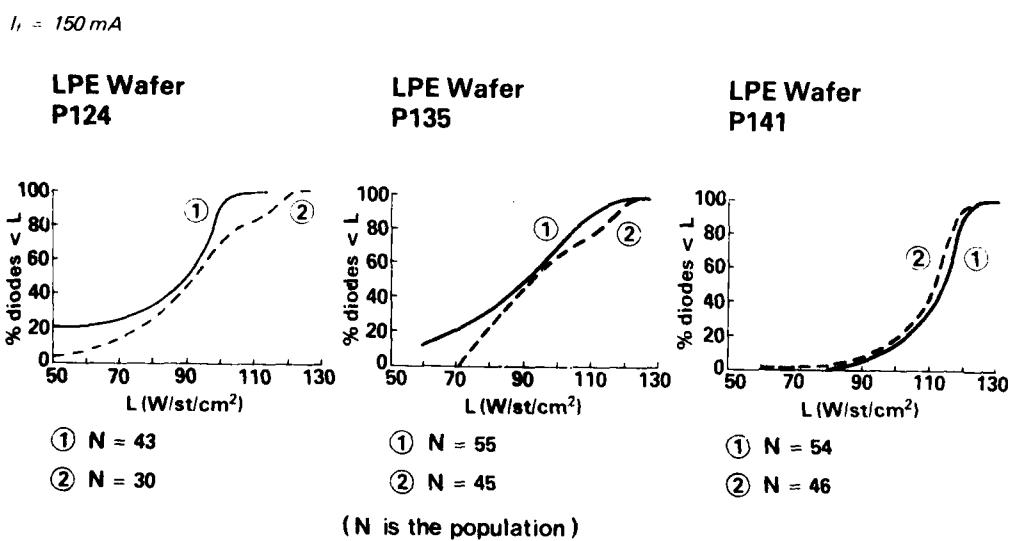


Figure 9.2
Radiance ($I_f = 150\text{mA}$) Cumulative

distribution as shown in Fig.9.2. This method of data reduction is applied to all of the characterisation data accumulated during this development.

The data of Fig.9.2. clearly shows good wafer-to-wafer consistency of efficiency and also good uniformity of efficiency within each wafer. We also observe no significant change in efficiency following power burn-in - any minor differences here can be ascribed to the different populations. (N is the population). For example the higher failure rate during burn in of low radiance devices from wafers P124 and P135 results in an increase in the mean batch radiance.

9.1.3. Forward and Reverse Voltages

Forward and reverse voltages are measured at 150mA dc and 100 μ A dc respectively using a conventional arrangement shown in Fig.9.3. As with radiance the measurement is incorporated in the CCTV inspection system. The cumulative distributions for these parameters given in Fig.9.4 show minimal changes have occurred during burn-in.

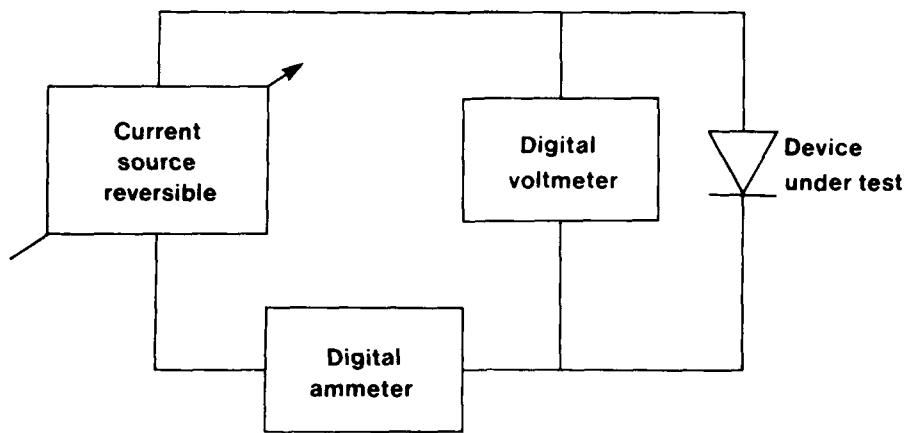
9.1.4. Pulse Response

Rise and fall time measurements are made using the apparatus outlined in Fig 9.5. The same arrangement is used for measuring pulse response times of pigtalled devices.

Distributions of results for t_r and t_f are shown in Fig.9.6. The excursions to longer fall times after burn-in for wafers P124 and P135 are probably due to minor differences in setting up the rather critical avalanching voltage of the detector. Later measurements on P141 and on pigtalled devices were somewhat more reproducible.

9.1.5. Thermal Resistance

Our measurement of thermal resistance (R_{th}) is based on the temperature dependence of optical power output. The diode is pulsed on for 0.5 sec



TPPD 5.3 and 5.4

Figure 9.3
Forward and Reverse Voltage (V_F, V_R)

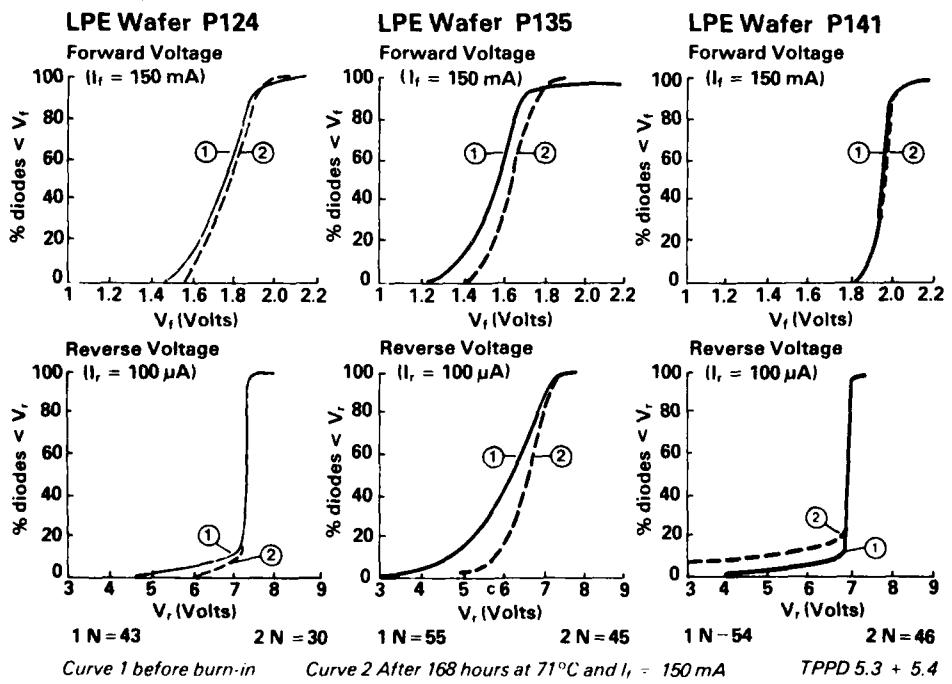
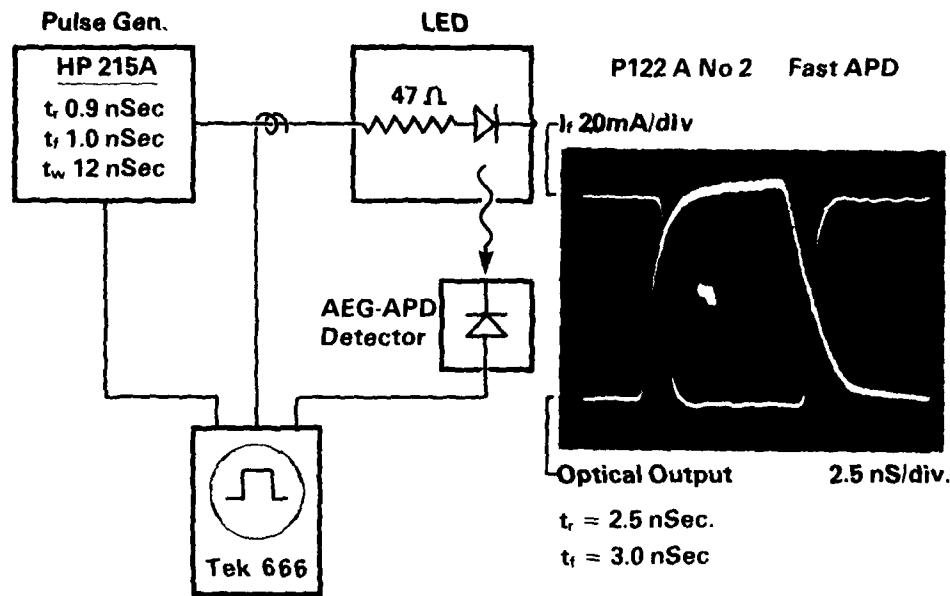


Figure 9.4

Forward and Reverse Voltages - Cumulative



(TPPD 5.5.1)

Figure 9.5

Pulse Response

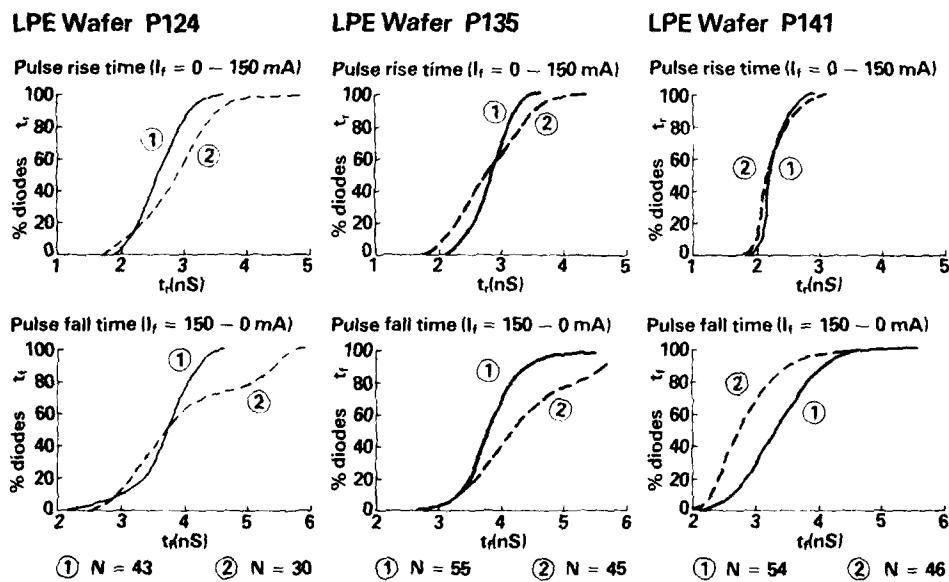


Figure 9.6

Pulse Rise and Fall Times Cumulative

at 150mA and the pulse repeated at 1 second intervals with the stud held at $> 25^{\circ}\text{C}$. The droop of light output is compared to the initial power out and R_s calculated as shown in the measurement schematic, Fig.9.7. Figure 9.8. shows cumulative distributions of R_s with median values consistently around $140^{\circ}\text{C}/\text{W}$.

9.1.6. Power Burn-In

Prior to lensing and pigtailing all diodes are submitted to a 168 hour, 71°C burn-in at the full rated current of 150mA. Following burn-in the diodes are again infra-red inspected and re-measured for L , V_F , t_r and t_f . At this point diodes showing large deviations from the pre-burn-in data are rejected. Also devices which exhibit dark defect formation in or near the active region are discarded, since such defects are known to propagate and cause premature device failures.

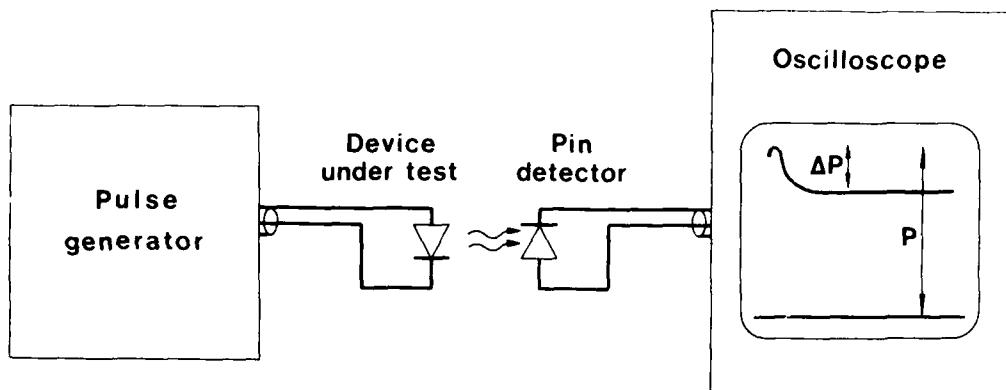
Junction capacitance is also measured following burn-in using a 1MHz capacitance meter with the LED unbiassed. The reduced data for C_j is shown in Fig.9.8.

9.1.7. Lensing

The power output of the device is measured into a free fibre both before and after lensing, using the method shown schematically in Fig.9.9. Fig.9.10. shows the reduced data and indicates an improvement in coupled power following lensing of between 7 and 9 times. The free fibre power was also used as an end-point measurement in the mechanical shock tests described in section 7. In addition, visual and infra-red inspections are made after lensing. This ensures that the lens is properly attached, has no blemishes and that the epoxy adhesive has formed a smooth continuous layer between the die and lens.

9.2. Tests on Pigtailed Devices

Diodes were pigtailed following the procedures outlined in section 4 and



$$R_e = \frac{\Delta P \times 100}{P \cdot V_F \cdot I_F \cdot T_C} \quad \text{where } T_C = \text{temperature coefficient of power output } (\%/\text{°C})$$

Figure 9.7

Thermal Resistance Measurement (R_e) TPPD (5.5)

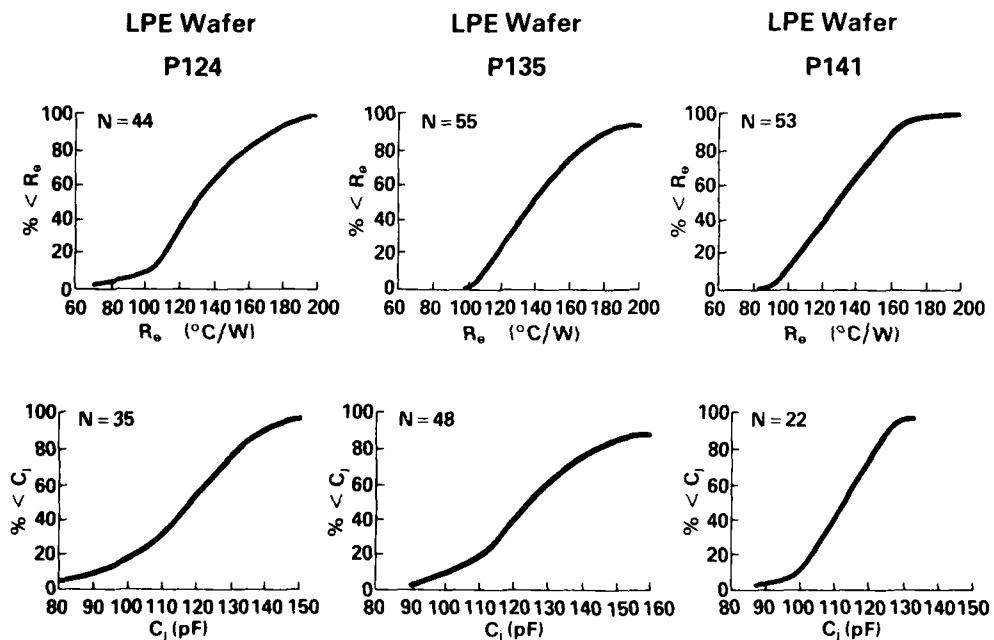


Figure 9.8

Thermal Impedance and Junction Capacitance Cumulative TPPD 5.5 and 5.12

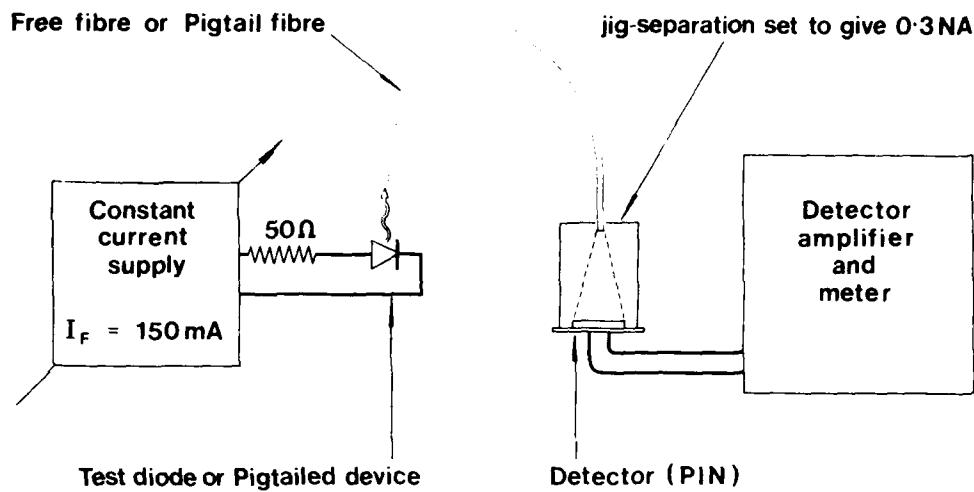
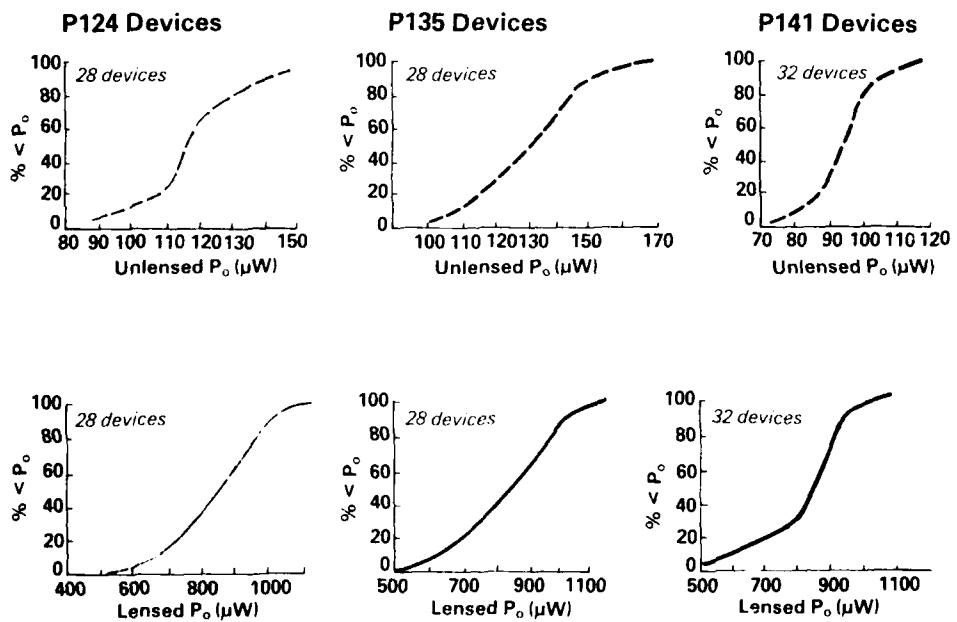


Figure 9.9

Power Out Measurement TPPD (5.8.1 & 5.8.2)



TPPD 5.8.2

Figure 9.10

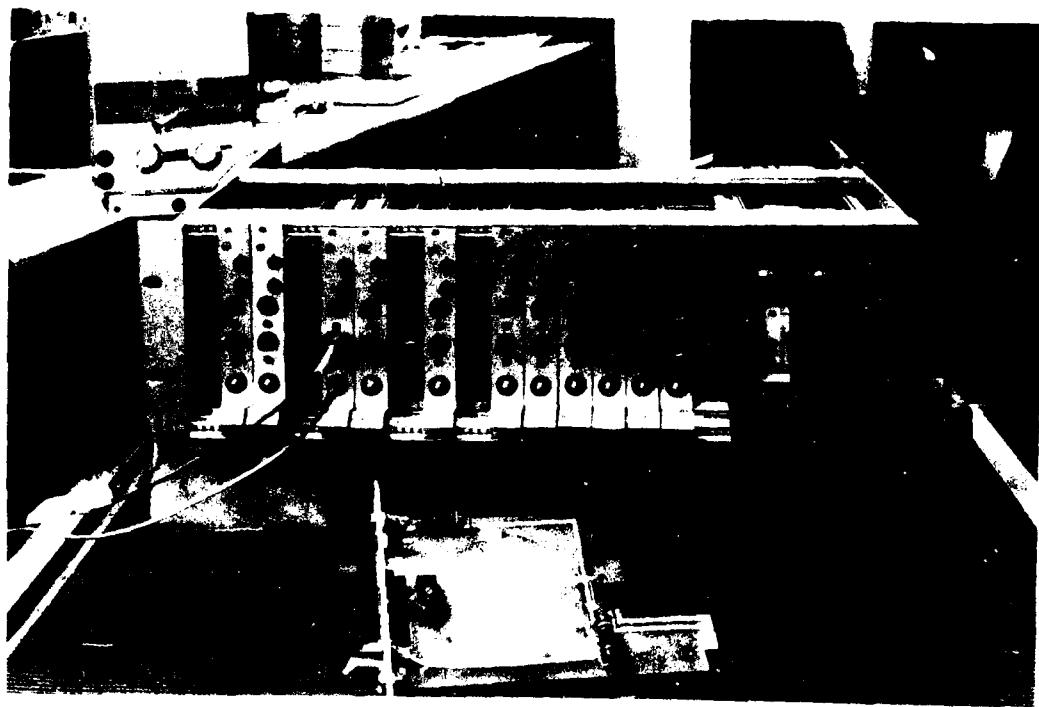
Power into Free Fibre (100μm Corning 0.3 NA) Cumulative

subjected to the test sequence detailed in the test plan of section 5 and Appendix A. The purpose of these tests is to provide full electro-optic characterisation data at temperatures of -55, +25, +71 and +125°C for the following parameters:-

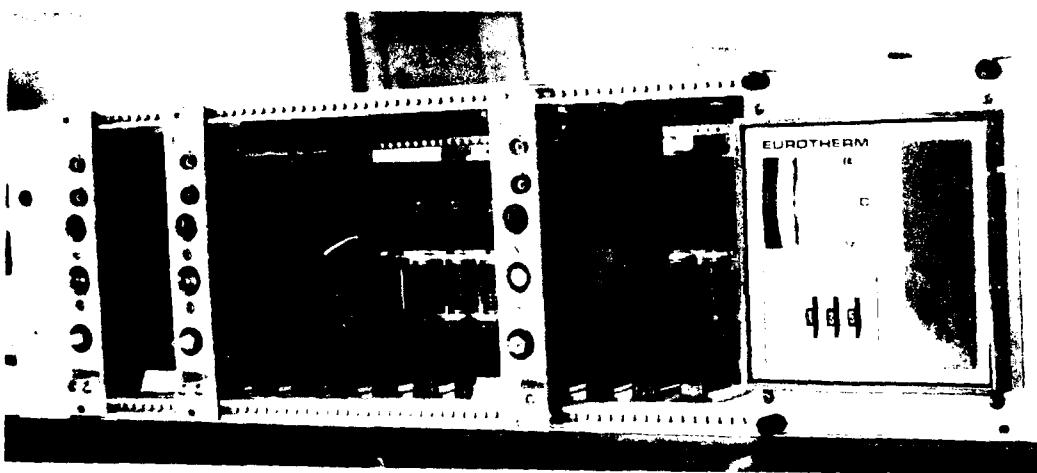
- a) P_o , optical power output d.c.
- b) P_o , optical power output, pulsed
- c) λ_p , peak emission wavelength
- d) $\Delta\lambda$, spectral emission half-width
- e) t_r , rise time of optical output
- f) t_f , fall time of optical output
- g) f_{3db} , modulation bandwidth
- h) V_F , forward voltage
- i) V_R , reverse voltage

In order to minimise handling of the pigtailed LEDs during this comprehensive test sequence a special characterisation test fixture was used.

Fig.9.11 (A & B) shows two photographs of the test fixture. In the foreground a pigtailed LED mounted in a heat sink block attached to a plug-in printed circuit board can be seen. The main frame has a temperature controlled bar running along the rear to which each heat sink is intimately coupled, as can be seen in Fig.9.11 (B). The pigtail of each device terminates in an optical coupling on the front plate of the plug-in which allows apertured optical power measurements or coupling through a fibre optic cable to remote measuring systems such as the spectrometer. Electrical input sockets are also provided on the front panel. The edge connector at the rear of the card is used in the life test station to supply 150mA d.c. constant current to the device. The total characterisation data collected on 33 pigtailed devices is presented in the reduced form in the series of Figs. 9.12 through 9.19. Also shown in this series are typical characteristics of P_o v I_f d.c. in Figs.9.13, P_o v I_f pulsed in Fig.9.14 and spectral characteristics in Fig.9.16.



(A)



(B)

Figure 9.11

Characterisation Testing Rig

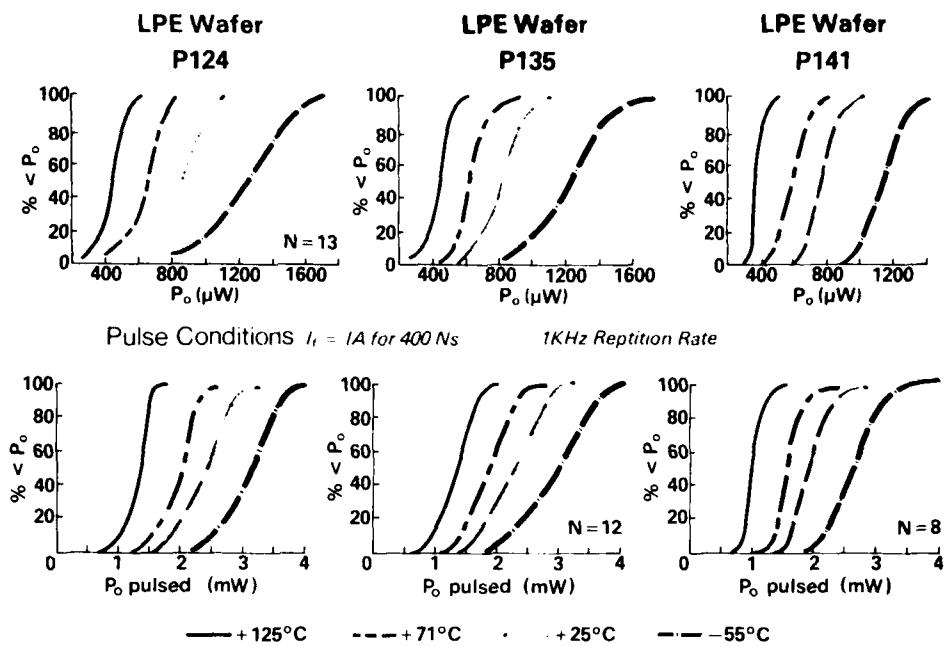
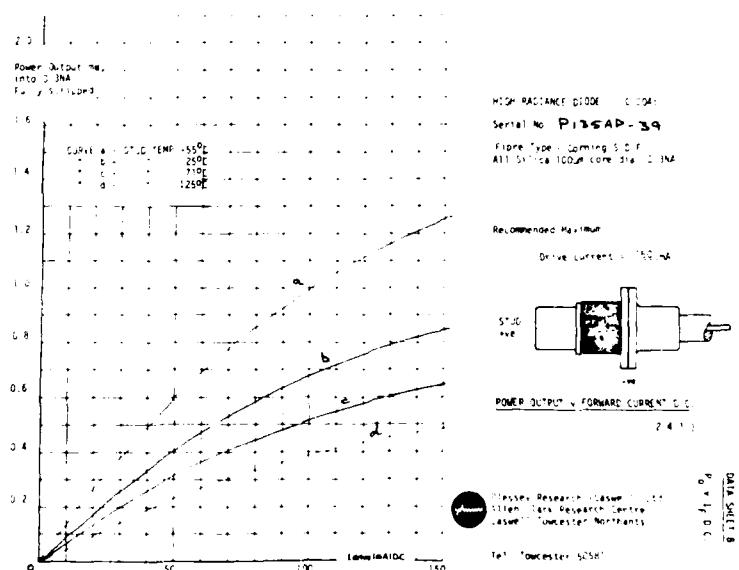


Figure 9.12

Characterisation Data Power Out and Pulsed Power Out - Cumulative TPPD 5.8.1



Data sheet 8

Figure 9.13

Typical Power Out Vs. Drive Current Data Sheet

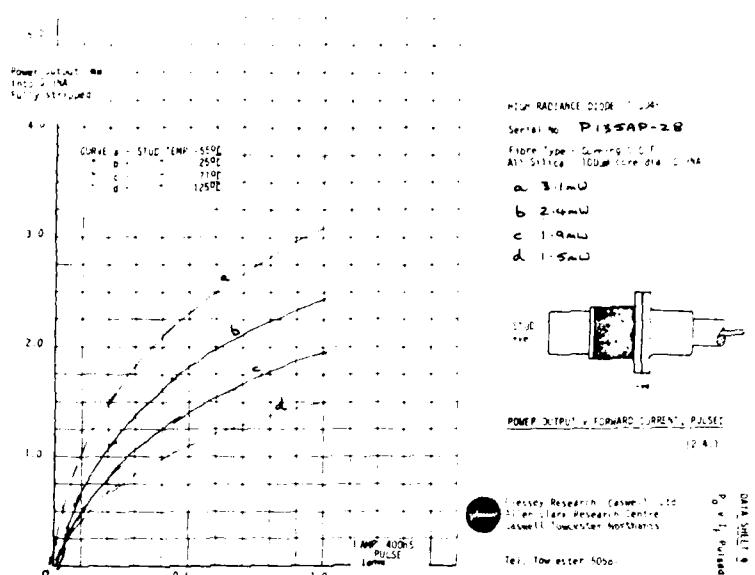


Figure 9.14
Typical Power Out v.s. Pulsed Drive Current Data Sheet

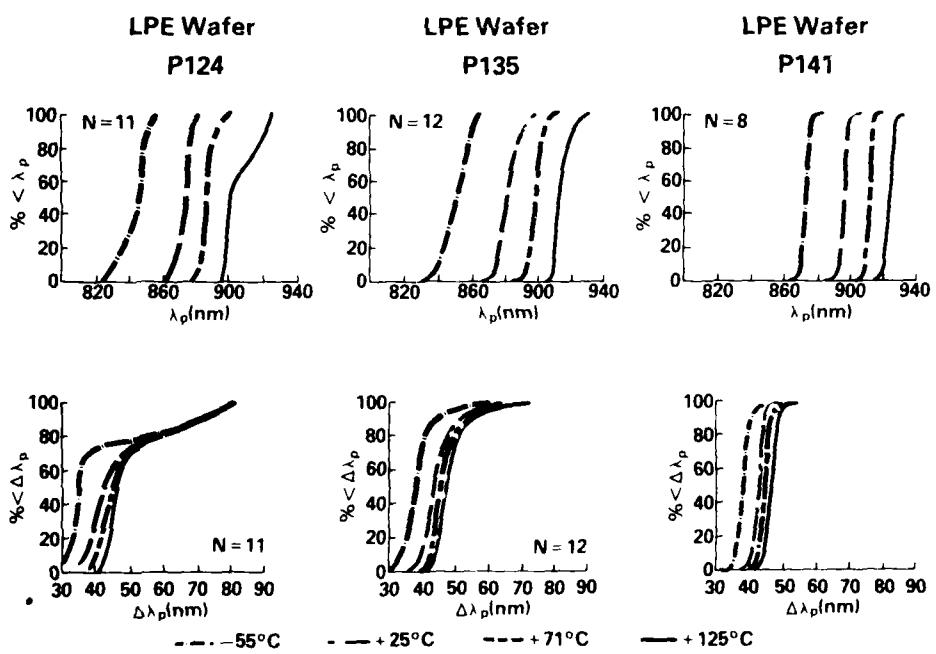
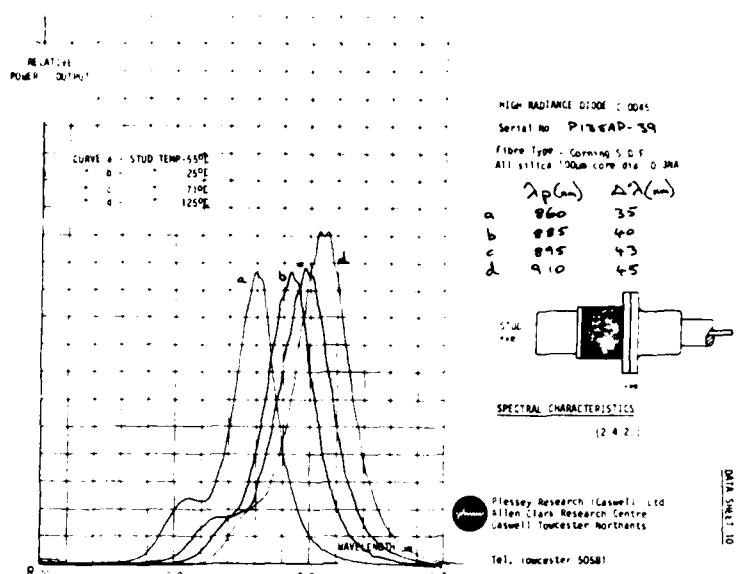


Figure 9.15

Characterisation Data Peak

Wavelength and Spectral Width - Cumulative TPPD 5.11



Data sheet 10

Figure 9.16
 Typical Power Out Vs. Wavelength Data Sheet

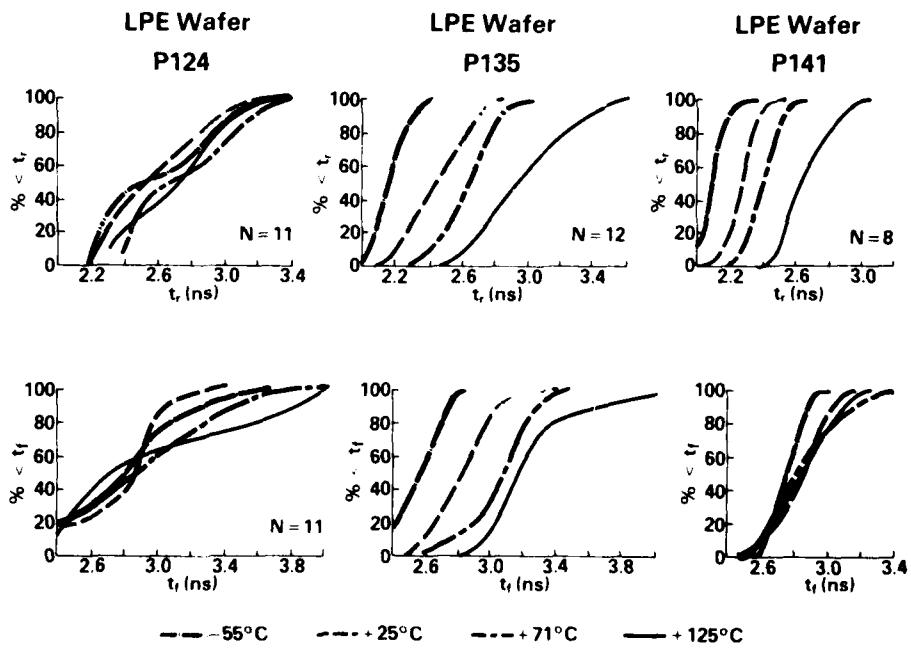


Figure 9.17

Characterisation Data Rise and Fall Times - Cumulative TPPD 5.6.1

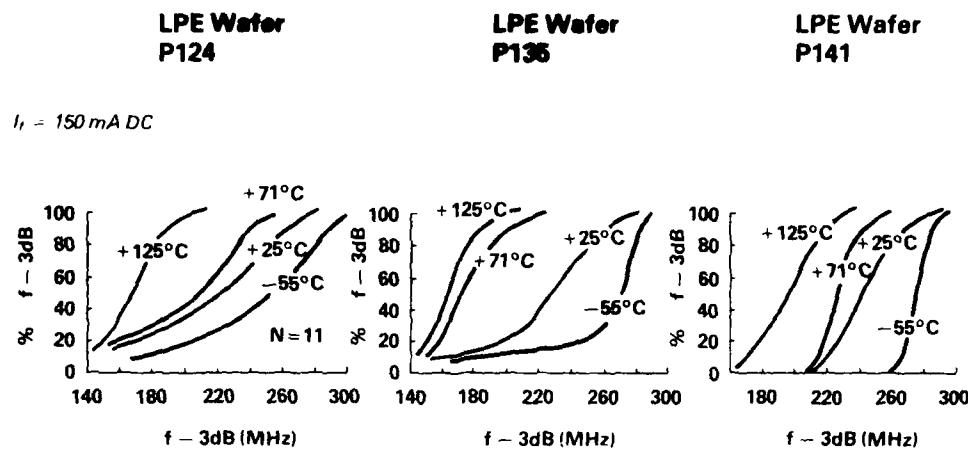


Figure 9.18
Characterisation Data Modulation Bandwidth Cumulative -
TPPD 5.6.2

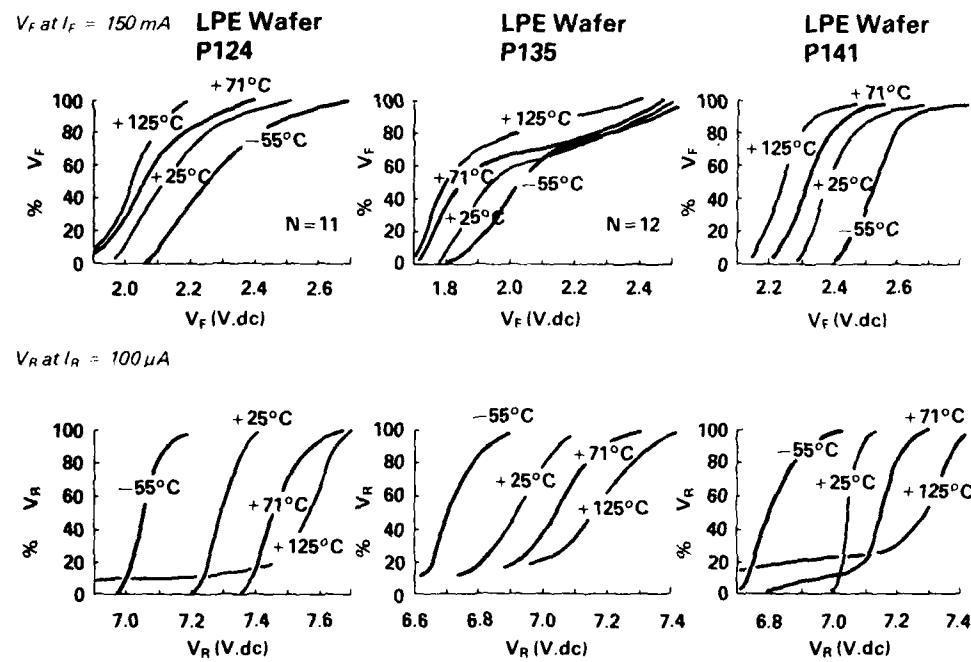


Figure 9.19
Characterisation Data
Forward and Reverse Voltage - Cumulative TPPD 5.3 and 5.4

The temperature dependence of the measured parameters is plotted in Figs.9.20 through 9.24. Here we have taken the median data from the cumulative plots at each of the measurement temperatures and for each of the three epitaxial wafers. The overall data is further reduced in Section 11 of this report, by summarising over all wafers to result in a total distribution from which characteristic data can be extracted.

9.3. Environmental Testing

9.3.1. Thermal Shock

Six pigtailed devices were submitted to 5 cycles of -55^0C for 30 minutes followed by $+85^0\text{C}$ for 30 minutes (MIL STD. 202E METHOD 107D Condition A). Power out checks on all devices and V_F , V_R measurements on two devices showed no failures. The same devices were then subjected to Condition B of the above standard (5 cycles, -65 and $+125^0\text{C}$ 30 minutes hold time) and re-measured for P_o , V_F and V_R . No significant changes in test parameters were observed except for a rise in forward voltage for one device (P135AP/52). The sequence of tests and the measured results are detailed in Table 9.1.

9.3.2. Mechanical Shock

Mechanical shock tests were made on pigtailed devices using the test jig described in section 7 for the testing of lensed diodes. Again 50G, 11msec and 100G, 6 msec shocks were applied axially and radially and also at temperatures of 25 and 125^0C . Table 9.2. summarises the test sequence and results, from which it is clear that the pigtailed devices are unaffected by these stress levels.

10. EXTENDED LIFE TESTING

In these tests devices are driven at their full rated current (150mA) at stud temperatures of 100 and 140^0C . The life testing facility is shown in Fig.10.1. and is of similar construction to the characterisation test fixture of Fig.9.11. A constant current of 150mA is supplied to the

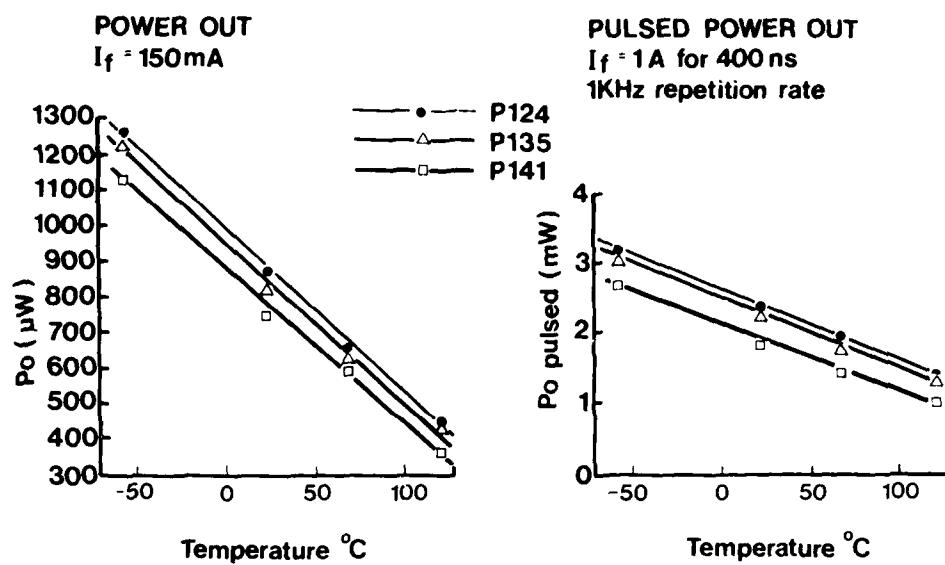


Figure 9.20
Temperature Dependence of Power Output

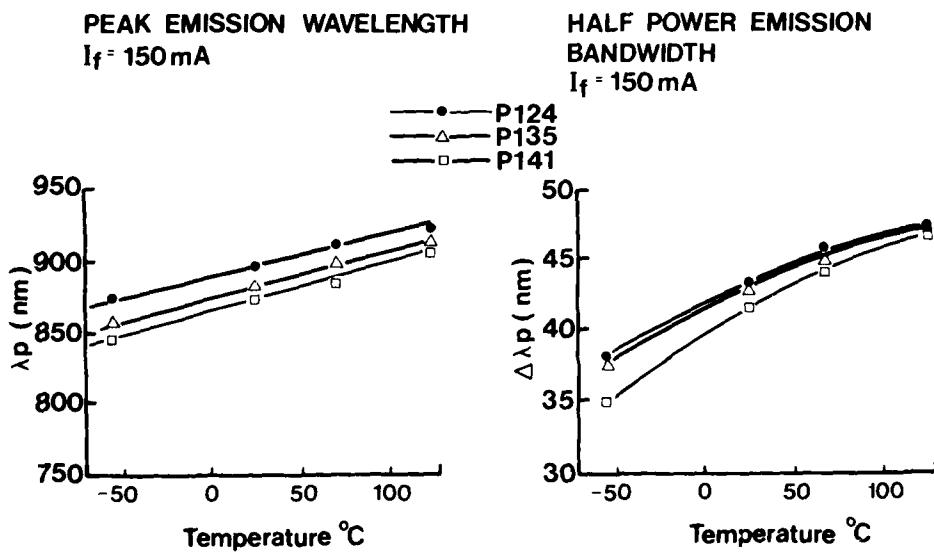


Figure 9.21
Temperature Dependence of Emission Wavelength

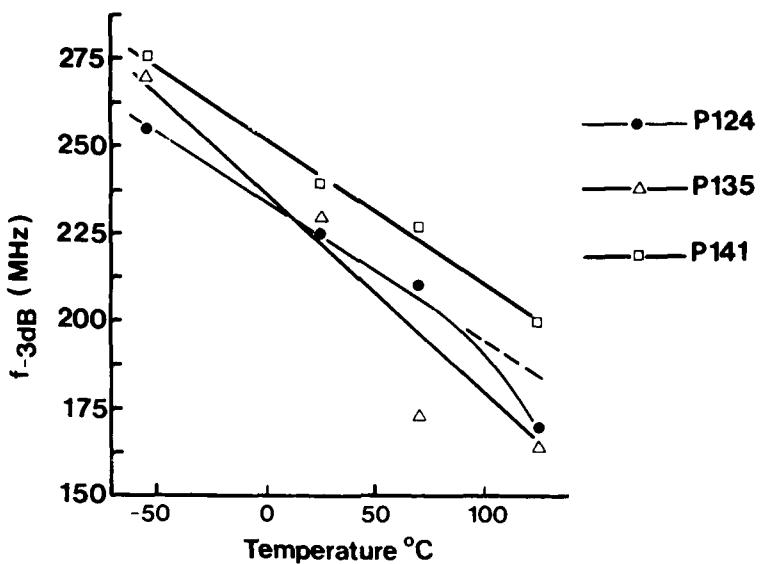


Figure 9.22
Temperature Dependence of Modulation Bandwidth

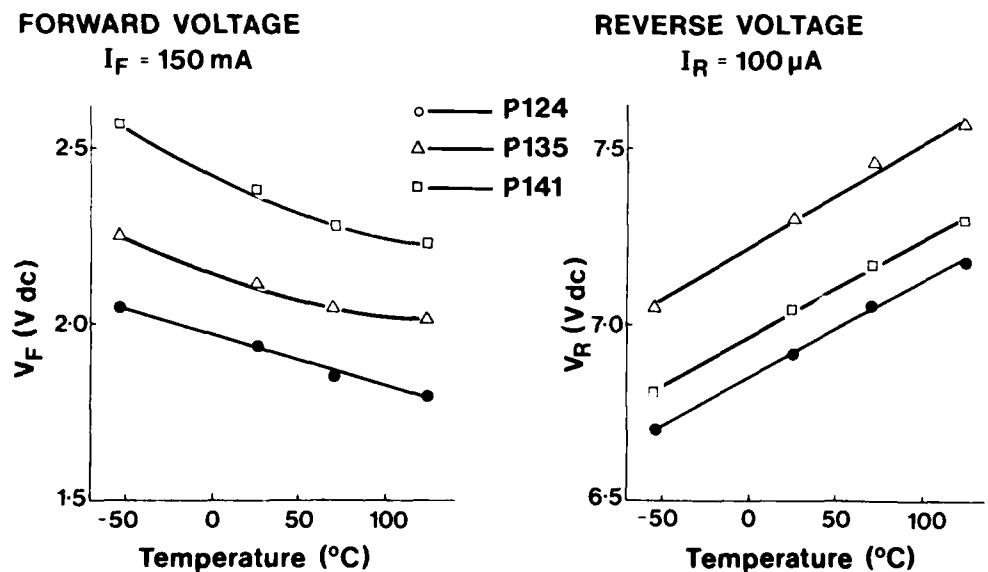


Figure 9.23
Temperature Dependence of Forward and Reverse Voltage

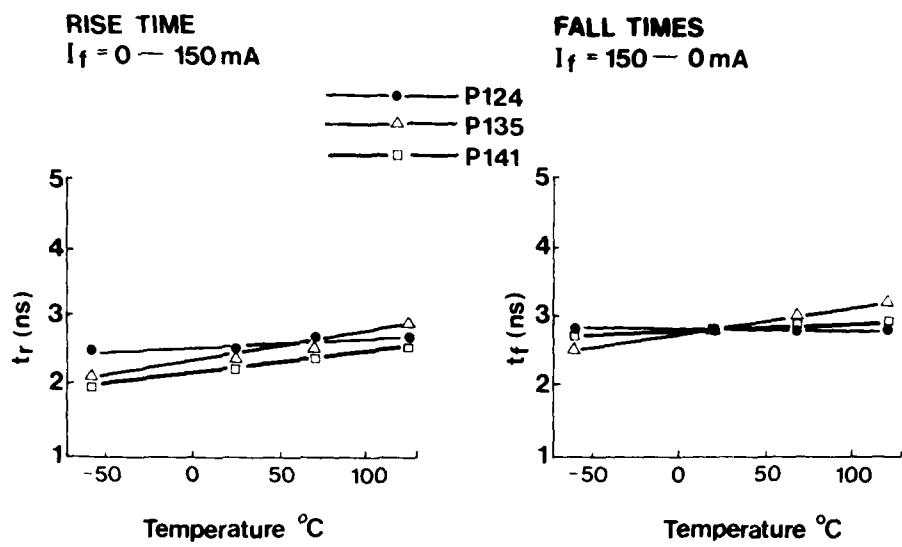


Figure 9.24

Temperature Dependence of Pulse Rise and Fall Time

TABLE 9.1

THERMAL SHOCK

INITIAL				After $-55 + 85^{\circ}\text{C} / 5 \text{ CYCLES}$			$-65 + 125^{\circ}\text{C} / 5 \text{ CYCLES}$			
Device No.	$P_o(\mu\text{W})$	$V_F(\text{V})$	$V_R(\text{V})$	$P_o(\mu\text{W})$	$V_F(\text{V})$	$V_R(\text{V})$	$P_o(\mu\text{W})$	$V_F(\text{V})$	$V_R(\text{V})$	
P141 AAP	44	513	2.40	7.04	532	2.38	7.01	494	2.37	7.03
"	49	532	2.61	7.01	532	2.59	6.98	532	2.58	7.00
"	36	846	2.31	7.08	893	-	-	893	2.39	7.09
P135 AP	51	786	1.77	6.93	817	-	-	798	1.78	6.99
"	52	665	1.80	6.89	684	-	-	703	2.43	6.96
"	56	1007	1.80	6.92	931	-	-	969	1.83	6.98

TABLE 9.2
MECHANICAL SHOCK

Device No.		INITIAL			POST 50g, 11mS Axial & Radial, 25 & 125°C	POST 100g, 6mS Axial & Radial, 25 & 125°C		
		Po(μW)	V _F (V)	V _R (V)		Visual Inspection	Po(μW)	V _F (V)
P141 AAP	44	542	2.38	7.08	✓	551	2.42	7.03
P135 AP	51	532	1.78	6.99	✓	532	1.8	6.90
"	52	532	1.8	6.96	✓	513	1.81	6.90
"	56	836	1.83	6.98	✓	855	1.96	6.93

device. The required device stud temperature is established by a temperature controlled bar as described in Section 9, page 44.

Fig.10.2. shows the progress of life tests at 100°C and 140°C on pigtailed devices up to 2,000 hours. The 50% failure point has not yet been reached for devices operating at 100°C whilst at 140°C the MTTF of the batch is ~ 1000 hours. Extensive life testing of GaAs homojunction devices has been carried out at Caswell (up to 52,000 hours actual running time at 35°C) and an activation energy of 0.55eV has been determined for such devices. Degradation in double heterojunction devices should follow similar processes and indeed an activation energy of 0.57eV has been determined by Yamakoshi et al (12). The 0.55eV figure provides acceleration factors of 74 and 388 respectively for 100°C and 140°C compared to 25°C . 1,000 hours at 140°C is then equivalent to $\sim 4 \times 10^5$ hours at 25°C and the 50% failure point at 100°C should occur at about 5×10^3 hours. These tests are continuing.

11. DEVICE CHARACTERISTICS AND SCREENING PROCEDURE

Looking firstly at the prime device parameters, Fig.11.1. shows the total cumulative data on power output, modulation bandwidth, and rise and fall times for the pigtalled devices fabricated. It can be seen that for each of these parameters the contract 'requirement' has been exceeded in 100% of devices and the contract 'goal' has been met 100% in terms of power output ($500\mu\text{W}$), 80% for modulation bandwidth (200MHz), 97% for rise time (3n sec) and 88% for fall time (3n sec).

The total cumulative plots for the secondary device parameters are shown in Fig.11.2. These are: forward voltage, reverse voltage, peak emission wavelength and spectral bandwidth. On peak emission wavelength 52% of devices fall within the contract requirement range of 0.82 to $0.88\mu\text{m}$.

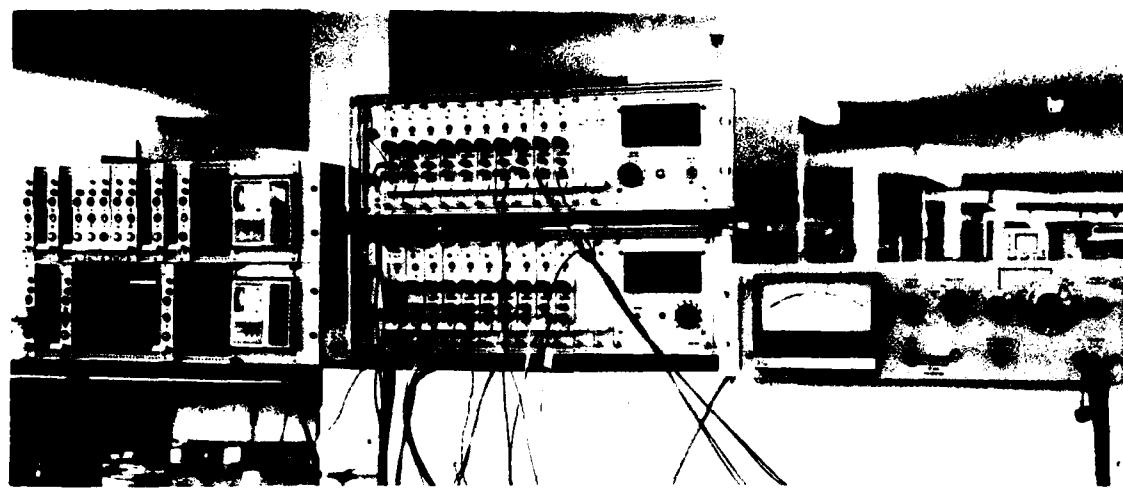


Figure 10.1
Photograph of Life Testing Station

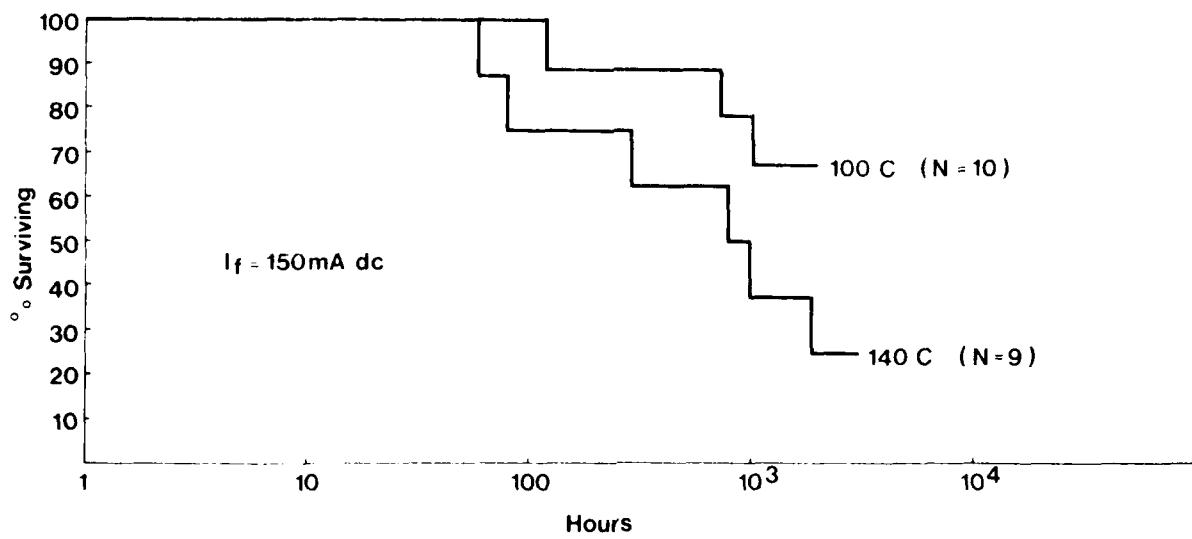


Figure 10.2
Life Tests at 100°C and 140°C

This can be corrected in future devices by a small increase in the aluminium level in the active layer. The other secondary parameters listed in 11.2 have no specified or required limits.

The overall collation of the cumulative parametric data is shown in Fig.11.3. in the form of a set of 25°C characteristics using the median data. Also shown are the parameter limits at the 10% and 90% distribution levels, and included where relevant the contract requirements and goals.

The screening procedure for deliverable devices is detailed in Appendix A and is designed to reveal critical parametric information about the LED under test in a rapid fashion. Fig.11.4 is a typical set of screening data as supplied with the deliverables. An initial set of 20 deliverables were screened in this fashion and delivered to AFWAL. These devices had characteristics typical of the data in Fig.11.3. and consequently about half of these devices have emission wavelengths outside the required 0.82 - 0.88 μ m range. A further 10 devices were assembled from the lower wavelength wafers and supplied to AFWAL to make a total of 20 devices meeting all aspects of the contract requirements.

12. SUMMARY AND CONCLUSIONS

The major objectives of this programme were met by extending our existing gallium arsenide / gallium aluminium arsenide double heterostructure materials technology to provide an LED source with the required speed-efficiency characteristics, and by enhanced optical coupling to the optical fibre pigtail by optimised microlens coupling techniques. Hermetic sealing of the fibre pigtail into the LED package was accomplished by our metallisation/solder method, additionally providing a rugged and stable device configuration.

To establish the double heterostructure layer configurations needed for high speed and efficiency a number of liquid phase epitaxy wafers were

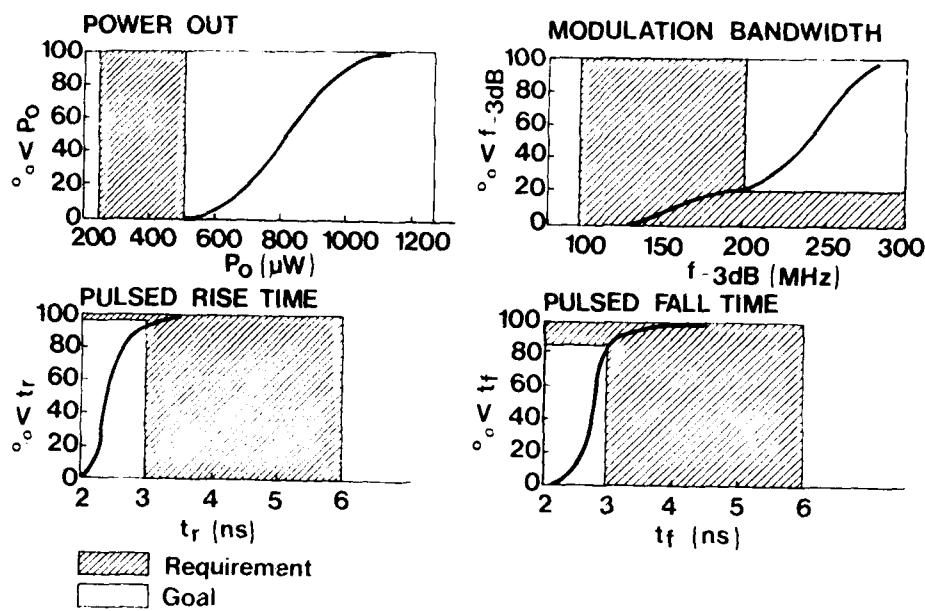


Figure 11.1
Summary of Pigtailed Device Data (1)

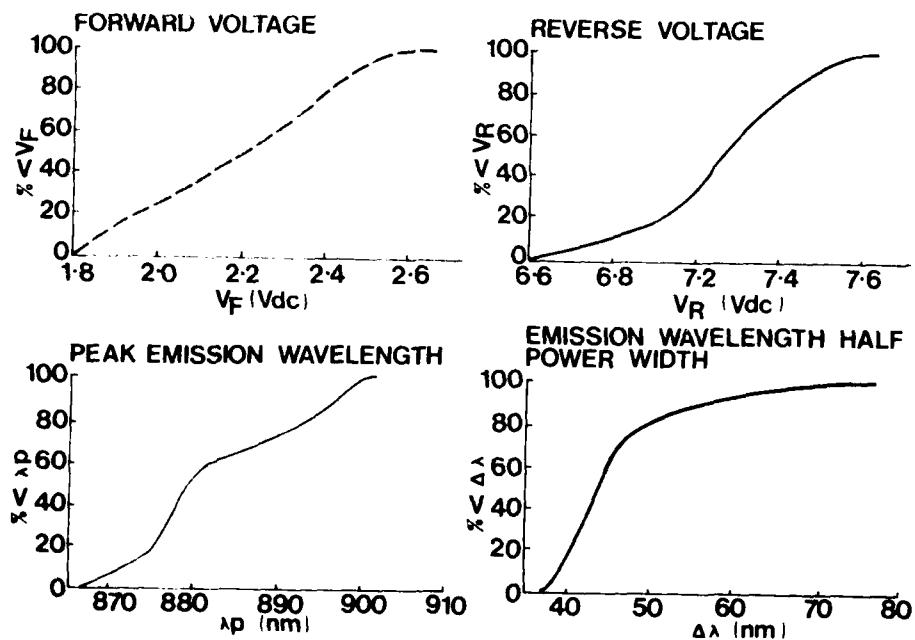


Figure 11.2
Summary of Pigtailed Device Data (For 25°C)

grown and processed into devices. These wafers had active layers of various thicknesses and doping levels, and devices were either oxide or proton bombardment isolated. We found that microlensed device efficiencies were sufficiently high in all wafers to launch the required power into the Corning SDF fibre. Consequently the final layer structure and emission area isolation technique were chosen to give the best speed. This final structure was proton bombardment isolated, had a $1\mu\text{m}$ thick active layer doped to approximately $4.5 \times 10^{18}/\text{cm}^3$ with germanium and containing 5% of aluminium. LPE wafers were prepared to this recipe for processing into pigtailed diodes and subsequent characterisation against the contract requirements.

Although we had developed a technique for fibre metallisation and solder sealing prior to this contract, considerable effort was needed here to demonstrate hermeticity to Military standards and to establish a procedure which would give good yields of sealed devices. We carried out the bulk of this work on stub fibred packages (no active chip included) and found that the major problem area was not in the soldered fibre seal, but in the basic copper-ceramic-kovar package assembly (S4 pill). These problems were overcome by improvements to the package, in conjunction with the manufacturer, and also by optimising the package welding procedures. Good yields of devices which maintained hermeticity after temperature cycling between -65 and $+125^\circ\text{C}$ were achieved.

Testing of pigtailed devices for hermeticity presented a further problem since in fine leak testing absorption and desorption of the ambient helium on the fibre plastic buffer coating gave rise to spurious leak indications. This effect varies markedly for different manufacturers pigtails. In the selected Corning SDF fibre the absorption was sufficiently low to allow satisfactory leak testing within the 30 minute delay period allowed by the test method detailed in MIL-STD-750B.

SYMBOL	PARAMETER	10%	MEDIAN	90%	REQUIREMENT	GOAL	UNITS
P_o	Power output	650	820	990	250	500	μW
t_r	Rise time (10-90%)	2.2	2.4	2.8	6	3	ns
t_f	Fall time (90-10%)	2.5	2.8	3.1	6	3	ns
$f_{-3\text{dB}}$	Modulation bandwidth (11mA p-p mod.current)	155	233	270	100	200	MHz
λ_p	Peak emission wavelength	872	879	897	(820-880)		nm
$\Delta\lambda$	Spectral bandwidth (Half power points)	39	43	57	—	—	nm
V_F	Forward voltage	1.86	2.18	2.45	—	—	V
V_R	Reverse voltage ($I_R = 100\mu\text{A}$)	6.8	7.1	7.3	—	—	V
R_θ	Thermal impedance	108	125	168	—	—	$^\circ\text{CW}^{-1}$
C_j	Junction capacitance ($V_F = 0$)	100	118	135	—	—	pF

Figure 11.3

Parameter Limits from Cumulative Data:

Case Temperature $T_C = 25^\circ\text{C}$ and Forward Current $I_F = 150\text{mA}$, Except where stated

PROVISIONAL SCREENING TEST

DEVICE NUMBER... P12449-45
Q.C. Inspection.....

Requirement or Test	TPPD C0045, CDRLA003		Symbol	Value	Units
	Method	Details			
<u>Die and Wire Bond</u>					
Inspection	5.1.1, 5.1.2.		-	✓	-
Radiance	5.2	$I_F = 150\text{mA}$	L	95	Wst-1cm^{-2}
Forward Voltage	5.3	$I_F = 150\text{mA}$	V_F	2.03	Vdc
Reverse Voltage	5.4	$I_R = 100\mu\text{A}$	V_R	7.34	Vdc
Thermal Independence	5.5		P_0	131	mW-1
Rise Time	5.6.1.	$I_F = 150\text{mA}$	t_r	2.5	ns
Fall Time	5.6.1.	$I_F = 150\text{mA}$	t_f	4.3	ns
Burn-in	5.7	$I_F = 150\text{mA}, 710^\circ\text{C}$ 168 hours	-	✓	-
Inspection	5.1.2.	I.R. emission uniformity		✓	
<u>Lensing</u>					
Inspection	5.1.2.		-	✓	-
Power output	5.8.2.	$I_F = 150\text{mA}$, Mode stripped, into 0.3NA	P_0	760	uW
<u>Pigtail and Seal</u>					
Inspection				✓	
Power output	5.8.1	$I_F = 150\text{mA}$	P_0	817	uW
Stabilisation Bake	5.9	1500°C, 24 hours	-	✓	-
Hermeticity	5.10	Fine, Gross 1 and Gross 2, MIL-STO-750B Method 1071		✓	
<u>Final Electro-Optic</u>					
Power output	5.8.1.	$I_F = 150\text{mA}, 0.3\text{NA}$	P_0	817	uW
Forward Voltage	5.3	$I_F = 150\text{mA}$	V_F	2.18	Vdc
Reverse Voltage	5.4	$I_R = 100\mu\text{A}$	V_R	7.32	Vdc
Q.C. Inspection			-		-

Figure 11.4

Sample of Screening Data for Deliverables

Erroneous gross leak indications were observed in fully assembled pigtailed devices. This was due to entrapment of the fluorocarbon test liquid within the pigtail stress relief assembly. We overcame this problem by leak testing all devices prior to affixing the stress relief structure.

Thermal shock tests were made on completed devices. No significant change in device parameters (power out, forward and reverse voltage) was observed in any of the devices submitted to 5 cycles, -55 to +85⁰C followed by 5 cycles -65 to +125⁰C (MIL-STD-202E Method 107D Conditions A and B). Mechanical shock tests were also carried out on completed devices, the conditions being 50G and 100G axial and radial shocks at 25 and 125⁰C. No changes were observed in any of the measured device parameters following this sequence of tests.

Extended high temperature life tests are being carried out. Here we are testing two batches of devices - at 100⁰C and 140⁰C at a forward current of 150mA d.c. A device is considered to be failed when its optical output has fallen by 3db and the median life of a batch is when 50% of the batch has failed. At 140⁰C we find the median life to be 1,000 hours. At 100⁰C the median life has not yet been reached after 2,000 hours of operation. From the 140⁰C test and assuming 0.55eV activation energy an extrapolated life of $\sim 4 \times 10^5$ hours is predicted. These tests are continuing.

A detailed characterisation and screening Test Plan was formulated in order to measure the parameters of the device which would be required for a formal specification in keeping with MIL-S-19500F. The provisional screening test was designed to be equivalent to conventional production and quality control testing of high quality MIL-Spec LED's.

Pigtailed LEDs were fully characterised at temperatures of -55, +25, +71 and +125°C. A summary of the 25°C characteristics extracted from this data is shown in Fig. 11.3. In this table we also show the contract requirements and goals for comparison against the measured device data where it can be seen from the median data that we have clearly exceeded the contract requirements and goals.

The overall conclusion here is that hermetically sealed, high performance pigtailed LEDs, which meet all the contract requirements and goals, have been developed and characterised to USAF approved levels, demonstrating clearly the soundness of the technical approach adopted.

Further work on this device should be aimed towards improvement of the established fabrication techniques in order to provide higher yields and lower costs of manufacture. These objectives could well be met within the scope of a Manufacturing Methods and Technology programme.

APPENDIX A

ENVIRONMENTAL TEST PLANS/PROCEDURES

1. SCOPE

The aim of this document is to describe in detail the proposed tests to be performed during the course of the programme. Four major categories of testing are planned and these are:-

- (a) characterisation testing (section 4.4.1. of SOW),
- (b) provisional screening testing (section 4.4.2. of SOW),
- (c) extended LED degradation tests (section 4.4.3. of SOW),
- (d) pigtail hermeticity.

The four categories of testing are detailed in the following sections of this report. The pigtail hermeticity testing is carried out as a separate early item in this test plan at the request of AFAL. Fig. 1 is a schematic representation of the Test Plan, indicating the sequence and the relationship of the tests to be carried out. Appendix A is the Programme Schedule Chart for the activities detailed in this TPPD.

2. CHARACTERISATION TESTING

The LED characterisation test plan is aimed at establishing the experimental device test requirements and detailed device characteristics. It is based on MIL standards and Plessey test procedures where appropriate. Upon completion of the 'p-n Junction Optimisation' (section 4.1. of SOW), thirty (30) devices will be fabricated from a minimum of three near optimal wafers for submission to the following test plan.

<u>ITEM</u>	<u>TEST (1)</u>	<u>PROCEDURE (see section 5 of this report)</u>
2.1. <u>Die Wire Bond</u>		
2.1.1. Inspection	Visual and I.R. inspection	5.1.1., 5.1.2.

<u>ITEM</u>	<u>TEST (1)</u>	<u>PROCEDURE (see section 5 of Appendix A).</u>
2.1.2. Electro-optic test	$L @ I_F = 150 \text{ mA}$ $V_F @ I_F = 150 \text{ mA}$ $V_R @ I_R = 100 \mu\text{A}$ R_θ $t_r, t_f @ I_F = 150 \text{ mA}$	5.2. 5.3. 5.4. 5.5. 5.6.1.
2.1.3. Power burn-in	168 hours @ 71°C and $I_F = 150 \text{ mA}$	5.7.
2.1.4. Inspection	I.R. inspection	5.1.2.
2.1.5. Electro-optic test	$L @ I_F = 150 \text{ mA}$ $L v I_F$ $V_F @ I_F = 150 \text{ mA}$ $V_R @ I_R = 100 \mu\text{A}$ $t_r, t_f @ I_F = 150 \text{ mA}$ $C_j @ V_F = 0, f = 1 \text{ MHz}$	5.2. 5.2. 5.3. 5.4. 5.6.1. 5.12.

2.2. Lensing

2.2.1. Inspection	Visual and I.R.	5.1.1., 5.1.2.
2.2.2. Electro-optic test	Power into free fibre	5.8.2.
2.2.3. Mechanical shock	Impulse at 25 and 125°C , 2-axis	5.14.1.
2.2.4. Inspection	Visual and I.R.	5.1.1., 5.1.2.
2.2.5. Electro-optic test	Power into free fibre	5.8.2.

2.3. Pigtail and seal

2.3.1. Electro-optic test	Power output, P_0	5.8.1.
2.3.2. Stabilisation bake	24 hours, 150°C	5.9.
2.3.3. Hermeticity	(a) gross	5.10.
	(b) fine	5.10.

<u>ITEM</u>	<u>TEST (1)</u>	<u>PROCEDURE (see section 5 of Appendix A).</u>
2.4. <u>Electro-optic (2) characterisation</u>	-55, +25, +71, +125°C	
2.4.1. Optical power output	(a) P_0 v. I_F D.C. (b) P_0 v. I_F pulsed	5.8.1.
2.4.2. Spectral characteristics	(a) λ_p @ $I_F = 150$ mA (b) $\Delta\lambda$ @ $I_F = 150$ mA	5.11.
2.4.3. Speed of response	(a) t_r @ $I_F = 150$ mA (b) t_f @ $I_F = 150$ mA (c) f_{3dB} @ $I_F = 150$ mA*	5.6.1. 5.6.1. 5.6.2. *(4)
2.4.4. Electrical characteristics	(a) V_F @ $I_F = 150$ mA (b) V_R @ $I_R = 100$ μ A	5.3. 5.4.
2.5. <u>Environmental</u>		
2.5.1. Thermal shock, temperature cycling	End point, V_F V_R and P_0	5.13.
2.5.2. Mechanical shock	End point, V_F V_R and P_0	5.14.2.
2.6. <u>Notes:</u>		
(1)	All symbols, except where indicated, are as recommended in MIL-S-19500 F, APP. 3.	
(2)	The intention here is to compile a matrix of device parameters as a function of temperature. Most of the parameters listed will be measured at the temperatures specified with the exception of modulation speed f_{3dB} and junction capacitance C_j . Data to be collated graphically is: L v I_F , P_0 v I_F , P_0 v f , P_0 v T , spectral response.	
(3)	P_0 is the symbol for optical power output from the free end of the pigtail fibre.	
(4)	f_{3dB} is the symbol for the modulation bandwidth as defined in 5.6.2.	

3. EXTENDED LED DEGRADATION TESTS

The objective here is to evaluate the reliability of the pigtailed device at elevated temperatures. Ten (10) pigtailed devices representing

the three selected processed wafers will be operated at 150 mA forward current at 100°C stud temperature and a further ten (10) devices at 140°C stud temperature. The optical output power of each device will be measured at intervals (see 5.7.). The tests shall continue until all of the diodes from each of the two batches have degraded by 3dB in optical power or until contract completion - whichever is the sooner. The time to half optical power output of each device will be recorded. In order to carry out these tests at 100 and 140°C, and also the Screening test burn-in at 71°C (see section 4), three lifetest jigs will be constructed.

4. PROVISIONAL SCREENING TESTING

The purpose of the Provisional Screening Testing Plan (section 4.4.2. of the SOW) is to reveal critical parametric information about the LED under test in a rapid fashion. It is intended that the twenty (20) deliverables called for will be screened according to this plan. The final structure of the Provisional Screening Testing Plan will depend to some extent on the results of the characterisation testing, but will follow the format outlined in Table 1.

TABLE 1
PROVISIONAL SCREENING TESTS

<u>REQUIREMENT</u>	<u>TEST CONDITIONS</u>	<u>TEST PROCEDURE</u> (See Section 5 of Appendix A)
<u>Die and Wire Bond</u>		
Internal visual	Die visual, I.R. inspection of emission uniformity	5.1.1., 5.1.2.
Initial electro-optic parameters	$L, V_F, t_R, t_f, R_\theta @$ $I_F = 150 \text{ mA}$ and $V_R @$ $I_R = 100 \mu\text{A}, 25^\circ\text{C}$.	5.2., 5.3., 5.6.1., 5.5., 5.4.
Power burn-in	168 hours, 71°C , $I_F = 150 \text{ mA}$ End point L and I.R. inspection	5.7., 5.2., 5.1.2.

<u>REQUIREMENT</u>	<u>TEST CONDITIONS</u>	<u>TEST PROCEDURE</u>
<u>Lensing</u>		
Internal visual	Lens visual, I.R. inspection of emission uniformity	5.1.1., 5.1.2.
Power output	Power into free fibre @ $I_F = 150 \text{ mA}$	5.8.2.
<u>Pigtail and Seal</u>		
Power output	P_0 at $I_F = 150 \text{ mA}$	5.8.1.
Stabilisation bake	150°C , 24 hours. End point P_0	5.9., 5.8.1.
Hermeticity	Fine and gross	5.10.
Power burn-in	168 hours, 71°C , $I_F = 150 \text{ mA}$ but may be omitted dependent on results of characterisa- tion testing	5.7.
Final electro- optic parameters	To specification	
Q.C. inspection		

5. PROCEDURES

5.1. Inspection

5.1.1. Visual die inspection

This inspection will be at a level to ensure good workmanship, both in the die preparation and also in the techniques used for die and wire bonding. The inspection will be carried out using a microscope set up for normal observation and illumination. Low magnification inspection will be at X50, as recommended in MIL-STD 750B, method 2072. High magnification inspection will be at X200. In view of the experimental nature of this programme, a record will be maintained of defects observed.

5.1.2 Infra-red inspection

This test is carried out to determine the uniformity of emission of the LED and also the number and form of dark defects within or near the emitting area of the LED. The LED is forward biassed at 1 - 10 mA and viewed using a microscope equipped with a suitable infra-red sensitive Vidicon. The LED emission is displayed on a CCTV monitor. The Z-modulation of a single line scan is also displayed for determination of emission intensity distribution.

5.2. Radiance (L, W/st/cm²)

Here, a magnified image of the LED is sampled by a small area PIN photodiode of known sensitivity. If the transmission factor T of the optical system is known, then:-

$$L = \frac{P}{A \cdot \Omega \cdot T} \quad \text{W/st/cm}^2$$

where P and A are the power received by, and the area of, the photodiode, and Ω is the solid angle subtended by the optical system at the photodiode.

5.3. Forward Voltage (V_F volts)

See MIL-STD-750 B, Method 4011.3. The device, clamped into a suitable heat sink, will be biassed in the forward direction at 150mA, the current being derived from a constant current source. The voltage across the device will be measured using a digital volt-meter.

5.4. Reverse Breakdown Voltage (V_R, volts)

See MIL-STD-750 B, Method 4021.2. The device will be biased in the reverse direction at 100 μ A, the current being derived from a constant current source. The voltage across the device will be measured using a digital volt-meter.

5.5. Thermal Resistance (R_θ, °C/W)

See MIL-STD-750 B, Method 3151. In the Plessey method, the temperature sensitive parameter is the optical output of the LED. The LED is pulsed on for 0.5 seconds, long enough for the junction to achieve thermal equilibrium. The fractional drop in optical output during this pulse is related to the junction temperature rise. A previous calibration, either on the device under test, or on a batch sample, gives the required relationship between temperature and optical output. During this test, the stud of the device is held at or near room temperature by clamping the stud into a suitable heatsink jig.

5.6. Speed of Response

5.6.1. Rise time, fall time (t_r , t_f , nSec)

The LED is pulsed at the specified current from a 50Ω source, via a 50Ω line and 47Ω matching resistor. No pre-bias or bias pedestal is used. The optical output of the LED is monitored by a fast, single response silicon APD operated well below saturation. The APD is terminated by a 50Ω resistor and connected by a matched line to a 50Ω input oscilloscope. The rise and fall times of the LED are determined by the 10 - 90% and 90 - 10% pulse transition times. Due allowance is made for the overall response of the system.

5.6.2. Modulation bandwidth (f_{3dB} , MHz)

The LED is operated at the specified forward bias current with a super-imposed peak-to-peak modulation current of 11mA. The modulation current is provided by a levelled, swept frequency source. The optical output of the LED is sampled by a single response Ge avalanche photodiode, the current from the photodiode after rectification being displayed as a function of frequency on a low speed oscilloscope. The frequency at which the modulated optical output has fallen by 3 dB relative to 1 MHz, is determined.

5.7. Power Burn-in

This test is performed to eliminate marginal devices or those with defects resulting from fabrication aberrations that are evidenced as time-and stress-dependent failures. Without the burn-in, these defective devices would be expected to result in early lifetime failures under normal use conditions. It is the intent of this test to operate the LED at specified conditions to reveal early failure modes.

During burn-in the LED is operated at 150mA forward current (D.C.) in a jig which maintains the stud of the device at 71°C for a minimum time of 168 hours. The optical output of the LED is measured at times $t_n \sim 2^n$ hours ($n = 0, 1, 2, \dots$). The test fulfills the requirements of MIL-STD-750 B, Method 1038, Test Condition B.

5.8. Optical Power Output (P_o , μW)

5.8.1. Pigtailed device

The pigtailed LED is placed in a jig which holds the stud at a known temperature and clamps the free end of the pigtail in a location groove against a thin glass plate at a fixed distance from a calibrated photodetector of known area. This distance is set so that the photodetector subtends the specified numerical aperture (N.A.). The specified forward current is applied to the LED. Prior to insertion in the location groove of the jig, the free end of the pigtail is stripped of all coatings over a 1 cm length and recoated with a high refractive index oil. This procedure effectively removes optical power coupled into the cladding of the pigtail. For D.C. operation the photodiode current is measured with a calibrated current meter. For pulsed operation the photodiode current is monitored using a suitable oscilloscope.

5.8.2. Power into free fibre

Here, the power output of a non-pigtailed LED is determined by locating a free fibre close to the emitting area, or lens, of the device. The fibre, generally of the same type to be fitted to the LED subsequently, is held such that the free end may be manipulated close to the LED. The fixed end of the fibre is held in the jig described in 5.8.1., so that the core optical power output of the fibre into a fixed N.A. may be determined.

5.9. Stabilisation Bake

This test is intended as a conditioning treatment and follows the procedures required by MIL-STD-883 B, Method 1008.1, Test Condition C.

The device shall be stored at the specified ambient temperature of 150°C for a period of 24 hours in a controlled temperature chamber capable of maintaining the specified temperature.

In the characterisation testing sequence this test is intended as a pre-conditioning treatment, with no specified and point measurements. In the screening tests the end point measurements will be optical power output (P_o).

5.10. Hermeticity

This test will be carried out as detailed in MIL-STD-750B, Method 1071, Test Condition H for fine leaks and Test Condition C for gross leaks.

In the first leak test the tracer gas shall be commercially pure helium. The bomb pressure shall be $60 \text{ psig} \pm 5 \text{ psig}$ and exposure time shall be 4 hours minimum. All devices shall be tested with a helium leak detector within 30 minutes after removal from the pressure chamber. Devices which exhibit leak rates greater than $5.0 \times 10^{-8} \text{ atm cc/sec}$ shall be rejected.

In the gross leak test leaks greater than $10^{-3} \text{ atm cc/sec}$ will be sought using FC-43 indicator fluid at $1250 \pm 50^\circ\text{C}$, and leaks greater than 10^{-5} sec will be sought using FC-78 pressurised to 90 psi, followed by FC - 48 indicator fluid at $1250 \pm 50^\circ\text{C}$. In both cases if a single bubble is observed devices are considered rejects.

For devices with plastic sleeved pigtails, desorption from the cladding materials is an unknown quantity and may well lead to an uncertainty in defining the acceptance levels for these tests.

5.11. Spectral Characteristics

Here, the relative output power of the LED is determined as a function of wavelength. The LED is operated at the specified forward current and the optical output from the pigtail is monitored by a spectrometer. The peak emission wavelength and the half-power linewidth are determined. The LED is held in a jig so that the specified stud temperature can be maintained.

5.12. Junction Capacitance

See MIL-STD-750 B, Method 4001. In the Plessey method the capacitance of devices is measured at a frequency of 1MHz and with zero applied voltage bias using an R.F. capacitance meter with an open circuit voltage of 15mV.

5.13. Thermal Shock/Temperature Cycling

See MIL-STD-202E Method 107 D. The intention here is to subject pigtailed devices to Test Condition A (5 cycles, -55 to + 85°C) initially and record end point data. Devices which are still functional following Test Condition A will be subjected to Test Condition B (5 cycles, -65 + 125°C) and the end point data recorded as in 2.5.1.; no dwell at room temperature for either test condition, 30 minute dwell at the temperature extremes.

5.14. Mechanical Shock

5.14.1. Non-pigtailed LED

This test will be carried out to yield information on the integrity of the lens/chip bond and will be performed in accordance with MIL-STD-202 E, Method 213 B. The test conditions to be used are A and C which are respectively 50 and 100 g peak acceleration and 11 and 6 mSec pulse duration. Both axial and radial shocks will be applied, the axial pulse directed so as to result in a tensile stress between the lens and chip. The initial tests will be carried out at 25°C. The survivors will be subjected to a similar series of tests at 125°C.

5.14.2. Pigtailed LED

Here, we will subject the pigtailed LED to a test schedule similar to that outlined in 5.14.1, with the objective of testing the strength of the overall assembly, but specifically the pigtail mounting.

6. PIGTAIL HERMETICITY TESTS

The intention of this series of tests is to establish at an early stage in the programme the validity of our solder/metallisation approach to hermetic sealing.

6.1. Dummy pigtail devices will be assembled using our proprietary techniques.

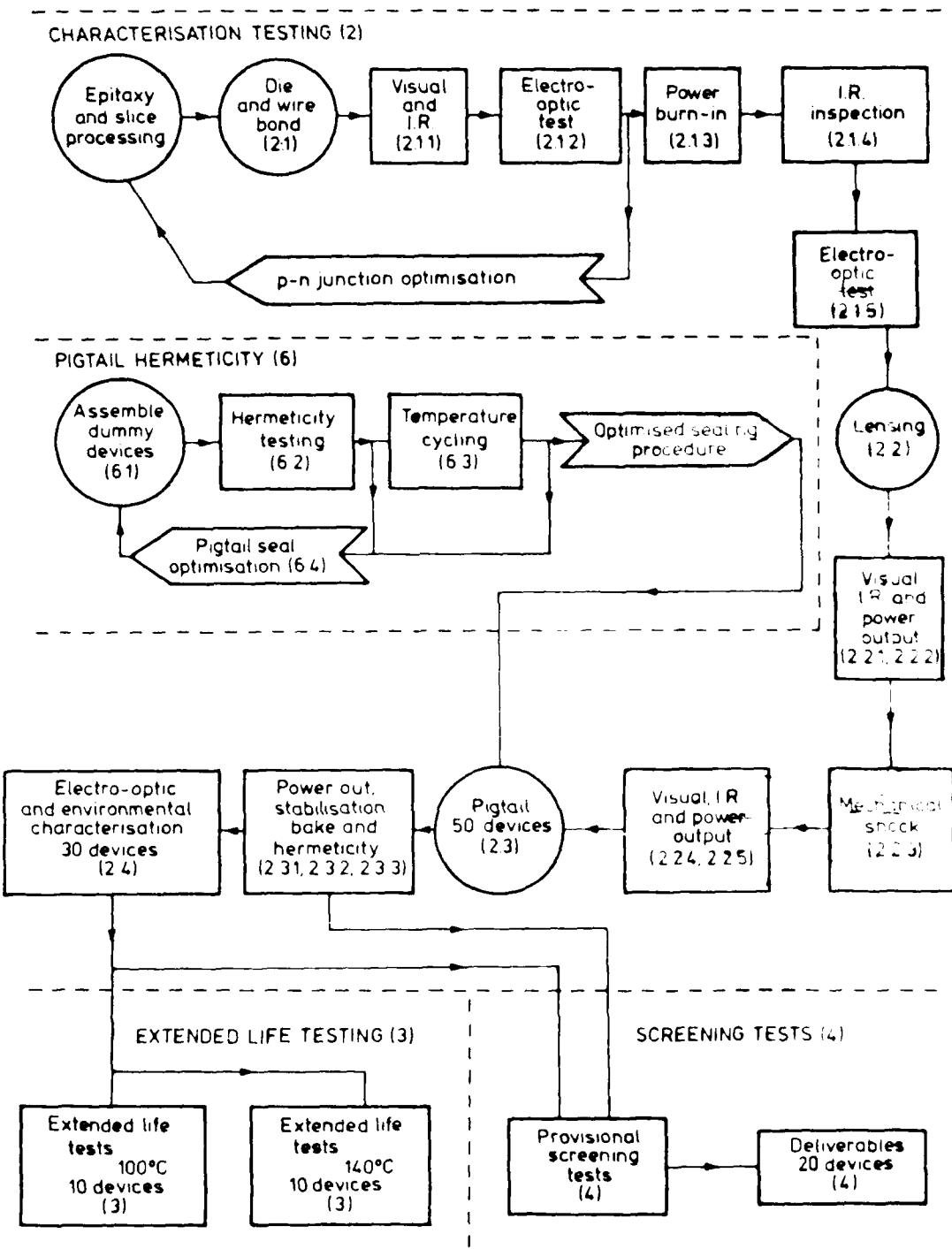
6.2. These dummy devices will be tested for hermeticity following the coarse and fine procedure detailed in MIL-STD-250 B (see section 5.10.). For these early tests high pressure Step 2 of Procedure C will be omitted.

6.3. Non-reject devices will be temperature cycled as in section 5.13. End point tests will be hermeticity as in 6.2. above.

6.4 A possible uncertainty in our pigtail seal relates to thermal expansion mismatch producing tensile interface stress between the primary and secondary metallisations. In the event of significant hermeticity failures being recorded in the above sequence of tests, our alternative course of action will be to adjust the properties of the secondary metallisation with the objective of minimising the tensile stress within the structure. Test devices will be fabricated in which either a stress-relieving layer or a thermal expansion match layer is included.

FIG A1

OUTLINE OF TESTING SCHEME



() numbers refer to paragraph in TPPD

PROGRAM SCHEDULE (PROJ) ILR 92CB		TITLE: Fibre-Optic LED for Avionics Applications												TYPE Test Plan		AS OF Aug 1979				
L I N E Ctr. #:	Contr: Plessey Research (Caswell) Limited PROGRAM MILESTONES	FISCAL YEAR 1979				FISCAL YEAR 1980				FISCAL YEAR 1981				FISCAL YEAR 1982				FISCAL YEAR 1983		
		MO	VR	ON	DI	FE	MA	J	AS	ON	DI	FE	MA	J	AS	ON	DI	FE	MA	J
1	CONTRACT																			
2	Die wire bond	(2.1)																		
3	Lensing	(2.2)																		
4	Mechanical Shock	(2.2.3)																		
5	Pigtailing	(2.3)																		
6	Electro-optic characterisation	(2.4)																		
7	Environmental	(2.5)																		
8	EXTENDED LIFE TESTS	(3)																		
9	SCREENING TESTS	(4)																		
10	HERMETICITY	(6)																		
11	Alternate procedures	(6.4)																		
12	DELIVERABLES																			
13																				
14																				
15																				
16																				
17																				
18																				
19																				

APPENDIX B - KEY PERSONNEL

R. Davis	- Programme Manager
R. Goodfellow	- Device Theory and Design
J. Ure	- Materials Technology
J. Humpage	- Processing Technology and Data Collation
M. Faultless	- Device Technology and Measurements

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